# Preliminary VFAT3 User Manual

V2.3

Preliminary draft version for internal use only

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1.   VFAT3: INTRODUCTION

1.1   General Introduction

This section is a brief summary of the main specifications of VFAT3 that are apparent to the user and relate to the physics performance of the GEM system. The most basic needs required by the project are summarized here:

• 128 channel chip
• Read positive or negative charges from the sensor
• Provide tracking and trigger information
• Trigger information: Minimum fixed latency with granularity of 2 channels
• Tracking information: Full granularity after L1A.
• L1A capability: L1A latency beyond 12.5 μs
• Time resolution of less than 7.5 ns (with detector).
• Integrated calibration and monitoring functions
• Interface to and from the GBT at 320 Mbps
• Radiation resistant up to 100 MRads
• Robust against single event effects

The block diagram for VFAT3 is shown in Figure 1.
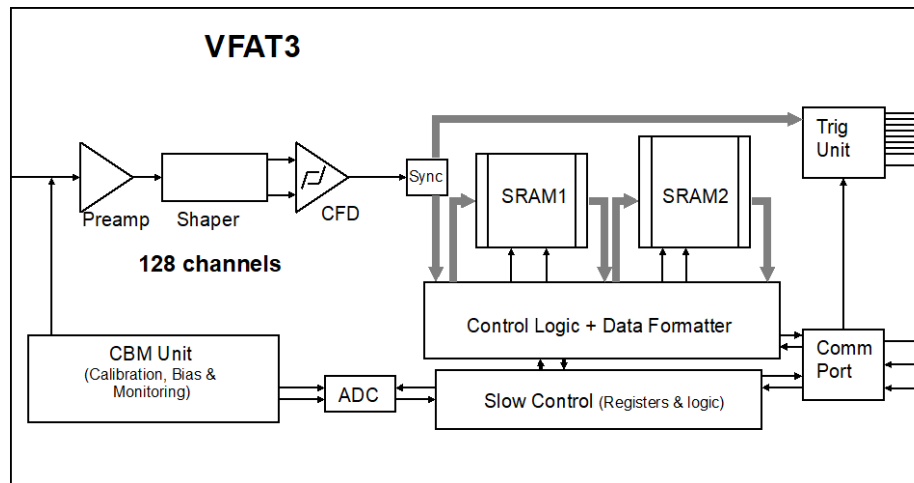
Figure 1: VFAT3 block diagram

VFAT3 is composed of 128 channels of charge sensitive preamplifier and shaper. This is followed by a constant fraction discriminator per channel. Following the discriminator is a synchronization unit which synchronises the comparator result with the 40MHz clock. The data then splits into two paths, one with a fixed latency for trigger signals, and the second for tracking data which is nonsynchronous. All communication with VFAT3 occurs through the Comm-port. This includes Slow Control commands and response as well as fast trigger commands, clock and calibration signals. The chip is highly programmable to offer maximum flexibility. This document contains the main design and user information needed to understand and use the chip.

1.2 The VFAT3 Analog front-end and timing resolution

The analog front-end is optimized for the readout of gaseous (and in particular GEM detectors) but could also be used to read out silicon detectors. The front-end Preamplifier and Shaper are programmable to offer flexibility when connecting to detectors of different capacitances and charge characteristics. Each channel contains internal input protection to offer robustness to charge (discharge) spikes. The frontend specification is shown in Table 1 and Table 2 including a list of the programmable options.

Signal charge from GEM detectors can last for approximately 60ns or so depending on the gas mixture. The shaping time of the front-end can be adjusted to fully integrate this charge and hence maximize signal to noise. Optimum timing resolution is maintained by the use of a CFD. Simulations show that the overall timing resolution can be maintained at around 5ns even with The maximum setting of shaping time. The gain is programmable to achieve optimum performance with 3 choices of dynamic range as shown in Table 2. DR10 is suitable for both GEM detectors and silicon detectors, DR30 and DR60 are suited to large area GEMs.

The calibration system provides internal charge pulses to the input of the of the front-end preamplifier. The magnitude, phase and polarity of the charge pulses are programmable. The channel to which the charge is injected is also programmable. This feature helps significantly in the production test and characterization stage as well as the detector setup and commissioning stage. The functionality has two modes, one which injects a quick charge pulse (similar to a delta pulse) and the second which injects charge via a constant current for a programmable length of time.

Table 1: Main specifications of the analog front-end

Key parameter	Comment
Detector charge polarity	Positive and Negative
Detector capacitance range	9 - 88 pF
Peaking times (T_p)	25, 50, 75, 100
Programmable Dynamic range (DR)	DR10, DR30 and DR60 (see additional table)
Linearity	< 1% of DR
Power consumption	2.5 mW/ch for pre-amp plus shaper
Power supply	1.2 V
Noise [DR10] _	1000e (with T_p=50 ns, C_d = 20 pF)
Technology	TSMC 130 nm CMOS

Table 2: Table of dynamic range (DR) settings. The table shows the DR upper limits and lower limit (noise floor).

Programmable Range Name	DR Upper Limit	Max noise floor at cd=10pF	Min Signal seen with S/N=20	DR
DR10	10fC	975e (0.156fC)	3.12fC	6b
DR30	30fC	1462e (0.234fC)	4.6fC	7b
DR60	60fC	1462e (0.234fC)	4.6fC	8b

1.3   The VFAT3 Variable Latency path (Tracking data path)

1.3.1   *Variable Latency path*

The block diagram for the variable latency data path is shown in Figure 2.
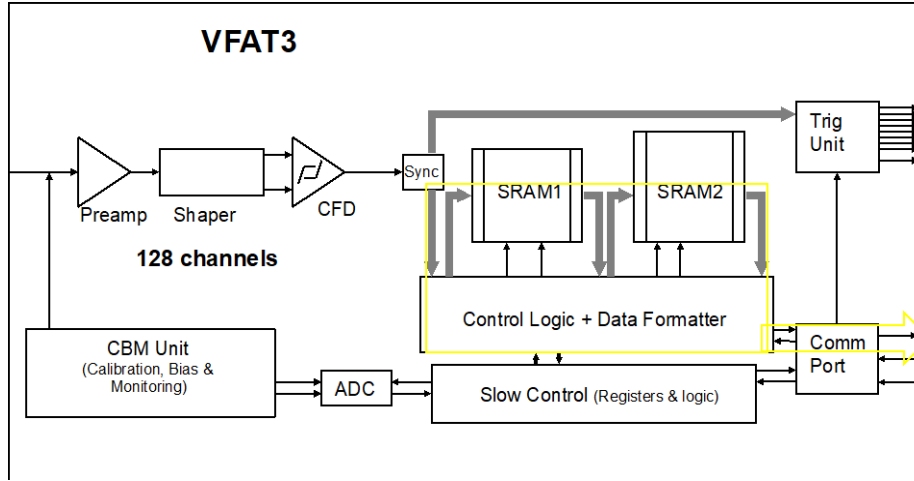
Figure 2 : VFAT3 block diagram indicating the variable latency path

This path is used for transmitting full granularity information via the Comm-port. The data is reduced in time by the application of a trigger arriving with a fixed latency. For operation in LHC for tracking data, this trigger is the LV1A. The data transmitted therefore has to be accompanied via a timestamp to identify the bunch crossing associated with the data.

1.3.2   *SRAMs and on-chip memory functionality*

The SRAM memories are sized to satisfy the LV1A maximum latency and rate specifications.

SRAM1 is a circular buffer continuously sampling all channels every clock cycle. It is 128 x 1024 bits which is 128 channels wide and 1024 deep. This means it stores data for all channels for 1024 continuous bunch crossings (bx) before looping around the buffer and overwriting previously written data.

SRAM2 is used for storing data from SRAM1 which are triggered via the LV1A signal which is received in the form of a control character (Table 16). In the experiment there is a fixed latency between the bx of interest and the LV1A signal. This is carried on into the internal operation of the chip and there is a programmable fixed time between the arrival of the LV1A CC and the time slot of data within SRAM1 which is transferred to SRAM2. Hence upon arrival of the LV1A CC, data corresponding to the bx of interest are transferred from SRAM1 to SRAM2 and time stamps are added. The VFAT3 LV1A latency is programmable, since SRAM1 is 1024 bits deep, the latency is programmable from 1bx-1024bx (Table 29). If only 1 timeslot of data is required per LV1A then the maximum programmable latency of 1024 corresponds to 25.6us.

SRAM2 acts as a FIFO. Data is added on receiving LV1A characters. Data is popped out sequentially and fed to the Data Formatter for Data Packet construction and transfer off chip. Data packets are hence queued within SRAM2 which means a variable latency path for the data transmission. The size of SRAM2 is 176x512. The depth of 512 corresponds to the maximum number of timeslots of data than can be simultaneously stored (queued) waiting for transmission off chip.

If SRAM2 becomes full, then further writing of SRAM2 is disabled until a free space is liberated and data corresponding to those triggers are lost. The EC counter continues to be incremented however so that when a space is liberated and new data written the time tags correspond correctly to written data.

Note : VFAT3 is capable of triggering on successive 40MHz clock periods. It is therefore possible to readout more than one timeslot per event. To do this the DAQ needs to produce multiple successive VFAT3_LV1A characters per one CMS LV1A signal. In this case however, VFAT3 would increment the EC for each VFAT3_LV1A hence the DAQ would need to keep a track of this.

1.3.3   Introduction to Data Formats

For the variable latency path there are two Data Types. The first is Lossless which is used to transmit full granularity information. The second is SPZS (Sequential Partition Zero Suppression) which has reduced size but can give losses in high occupancy environments. An important concept for the data packet description is the use of Control Characters (CC) as headers. All commands are delivered to the chip via control characters of 8 bits long. Each one unique and representing an individual command such as LV1A, ReSync etc. Data packets sent from the VFAT3 use CC as headers of the different type of data packets.

Data Type: Lossless
The lossless data packet style is derived from the VFAT2 data packet but is optimized in terms of content. A unique CC acts as a header identifying the start of the packet. The timestamp is included in the form of the EC and BC numbers. The Hit data is represented by one bit per channel, a logic 0: represents no-hit and a 1 represents a hit. If 1 or more channels are hit then there is no further attempt to zero suppress. The final piece of information is the CRC to confirm the integrity of the data packet.
It is possible to suppress the BC time tag if only the EC is required. It is also possible to suppress the entire data field if no channels are hit. Indeed, a further possibility is to suppress the entire data packet if no hit is registered and transmit only a control character.
It gives flexibility for the DAQ system to decide if it requires all VFAT3s to operate synchronously sending data packets regardless of their content or to have a data driven operation where data packets are sent only when registering hits. Since most of the chips will record nothing in any given bunch crossing the latter option optimizes bandwidth enormously. Each chip however, even in the minimum setting, will respond to a LVA1 trigger by sending at least a Control Character to acknowledge receipt of the trigger signal and transmit the information: no hits corresponding to this trigger.

The data field is transmitted MSB first, ie the first bit is channel 127 and the last bit is channel 0.

Data Type: SPZS (Sequential Partition Zero Suppression)
The SPZS style incorporates zero suppression and is a variant on the CMS RPC data format. In this case the size of the data packet is a function of the number of hits in the chip. This enables very small data packets and hence the highest possible data transmission rate. This is very good for operation at high trigger rate. The disadvantage is that for high occupancy some losses could be incurred.

The principle is as follows: The 128 channels is divided up into 16 partitions. Each partition contains 8 channels. For each event only the partitions containing data will be transmitted. If the overall occupancy is low, there will be a bandwidth saving on the payload transmitted per event. The maximum number of partitions per data packet is limited to a programmable limit. If more than the maximum number of partitions are hit then an Overflow occurs generating its own CC . Hits causing an overflow are lost.

1.4 The VFAT3 Fixed Latency path (Trigger path)

1.4.1 Fixed Latency path

The fixed latency path is highlighted Figure 3 .The purpose is to provide fast hit information which is synchronous with the LHC 40 MHz clock. The hit information can then be put in coincidence with other detectors (such as the CSCs) to build CMS muon triggers. There are 8 SLVS pairs running at 320MHz.
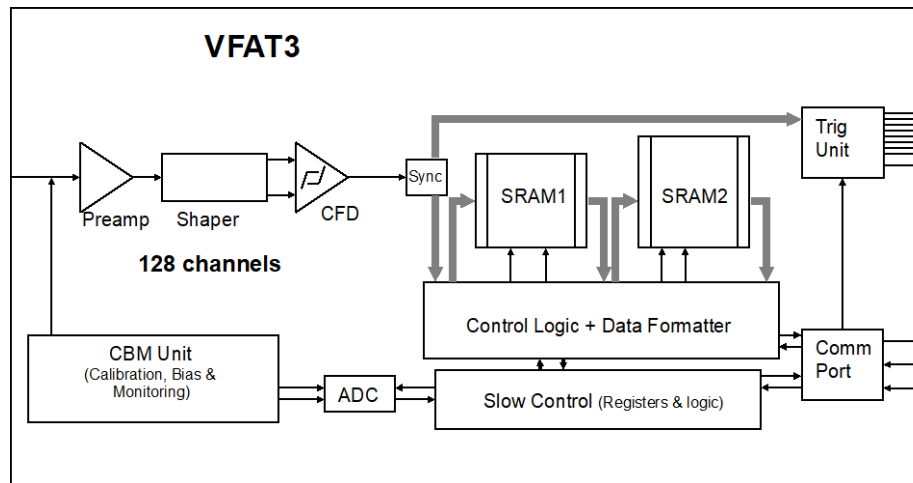
Figure 3: VFAT3 block diagram indicating the fixed latency path

These SLVS pairs can be configured to transmit either in Single Data Rate (SDR) or (Double Data Rate DDR) with the following granularities:

SDR	Fast OR information	8 x 8bits/bx = 64bits/bx for 128 channels	granularity = 2 ch
DDR	Full channel information	8 x 16bits/bx = 128bits/bx for 128 channels	granularity = 1 ch

The DDR uses both edges of 320MHz to transmit data.

1.5   Data Synchronisation and Pulse Stretching

The interface between the analog (asynchronous) front-end and the digital (synchronous) part of the chip is controlled by a data "Synchronisation and Pulse Stretching" block simply stated as "Sync" in the block diagram of Figure 1.

The signal pulse output of the front-end CFD is sampled and synchronised to an internal 40MHz clock. Also included in this block is Pulse Stretching logic that can stretch a synchronised pulse from 1 to 8 clock periods. The stretching of the pulse is only valid for the Variable Latency path. The Fixed Latency path uses synchronised pulses of one clock period only.

The synchronisation and pulse stretching block can work in either "edge" or "level" modes. The synchronisation mode and Pulse Stretching length is programmed by the "SyncLevelEnable" and "PS" fields of Table 21: GBL CFG CTR 0: Control Logic Settings .

The main difference between "edge" and "level" modes is the way the block treats the incoming asynchronous pulse from the CFD.

In "Edge" mode, the input pulse from the CFD is sampled on the rising edge of the internal 40MHz clock. The output from the block is a synchronised digital pulse with pulse length equal to the number of clocks set in the PS field. The output pulse length is independent of the CFD pulse length.

In "Level" mode the level of the CFD pulse is sampled every clock cycle and the "PS" pulse length added to that. Hence is the CFD output is N clock cycles long, the output of the synchronisation block is N+PS+1 clock cycles.

Figure 3, Figure 4, Figure 5 and Figure 6 show simulation results illustrating these differences.
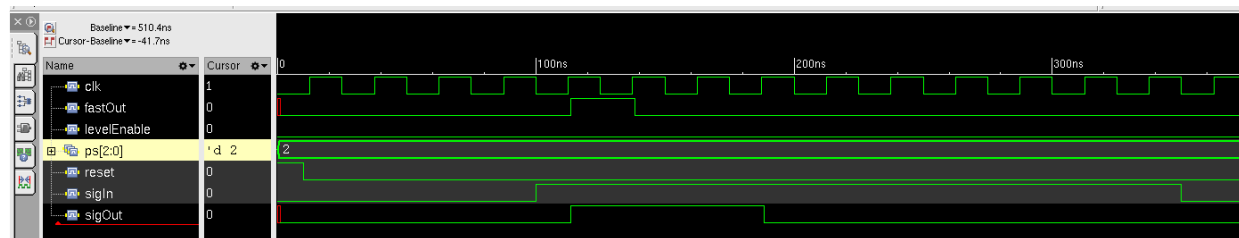
Figure 4: Edge Mode example 1, PS=2, CFD Pulse length = 250ns, Output signal is stretched but independent of the incoming CFD signal length.
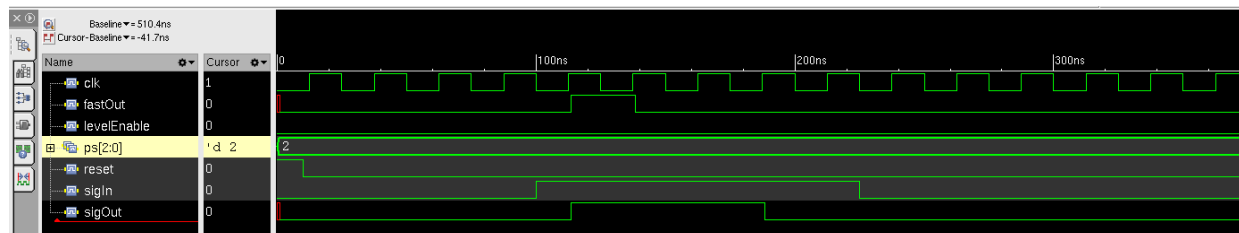
Figure 5: Edge mode example 2, PS=2, CFD pulse length = 125ns, Output signal is independent of the CFD pulse length.
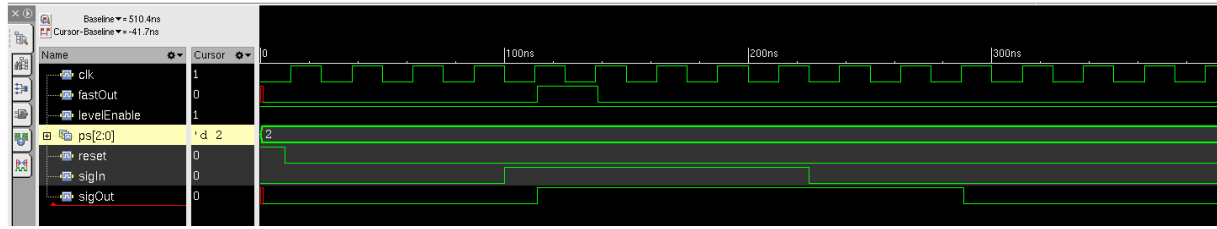
Figure 6: Level Mode example 1, PS=2, CFD pulse length = 125ns, Output pulse length is dependent of the CFD pulse length, output pulse = CFD pulse length + PS + 1.
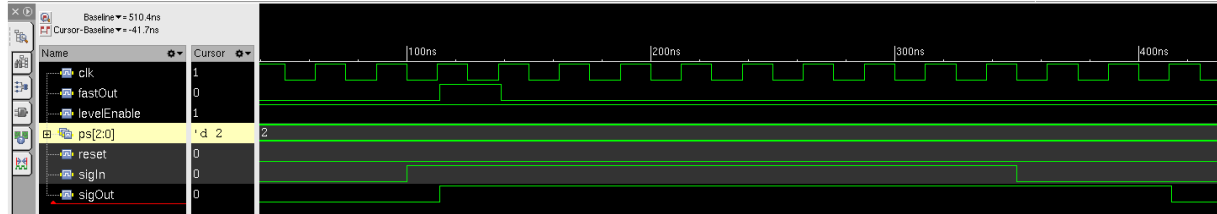
Figure 7: Level mode example 2, PS=2, CFD pulse length = 250ns, output pulse length = CFD pulse + PS + 1.

1.6   The VFAT3 Control Interface

The slow control allows the writing and reading of internal registers which in turn provides the functions of programmability and monitoring.
VFAT3 uses the Comm-port for all data communication including the slow control. The use of CC in the Comm-port allows slow control commands and data to be distinct from all other commands and data fields. This is achieved by having two slow control CC, one for communicating a slow control 0 and the other for writing a slow control one 1.

The slow control protocol adopts the IP-bus protocol (standard within CMS upgrades) and wraps this within the HDLC protocol. This ensures correct chip addressing and error checking of slow control packets. Reception and transmission of slow control commands/data must take low priority when compared to real data traffic. It is therefore possible to start and stop the slow control communication in mid flow and resume when the Comm-port is free. The maximum allowable slow control communication rate is 40Mbps.

1.7   The Operational Flow

VFAT3 has the more or less the same operational flow as VFAT2 and is shown in figure 4.
A Power-On reset signal puts the chip directly into SLEEP mode when the chip is powered up. This is a minimum power consuming stable state. This is achieved by having hard wired default values for the registers applied during SLEEP mode. During SLEEP mode all state machines are in their reset state, the only part of the chip which is awake is the Comm-port which is listening for commands. During SLEEP mode the Slow Control registers can be loaded with values. The values are not applied to the individual circuits of the chip however until the chip is placed in RUN mode. All programmed values can be read from the Slow Control registers during SLEEP mode to verify that the communication and writing of programmable settings worked correctly.
The chip can then be placed into RUN mode. This is achieved by changing the SLEEP bit from a 1 to a 0. At this point the analog bias settings are applied and the digital state machines start turning. The power consumption of the chip increases to its operating level.
Application of a ReSync signal aligns all SRAM write and read pointers and resets the time tag counters (BC and EC).
From this point onwards the chip is in synchronised RUN mode.
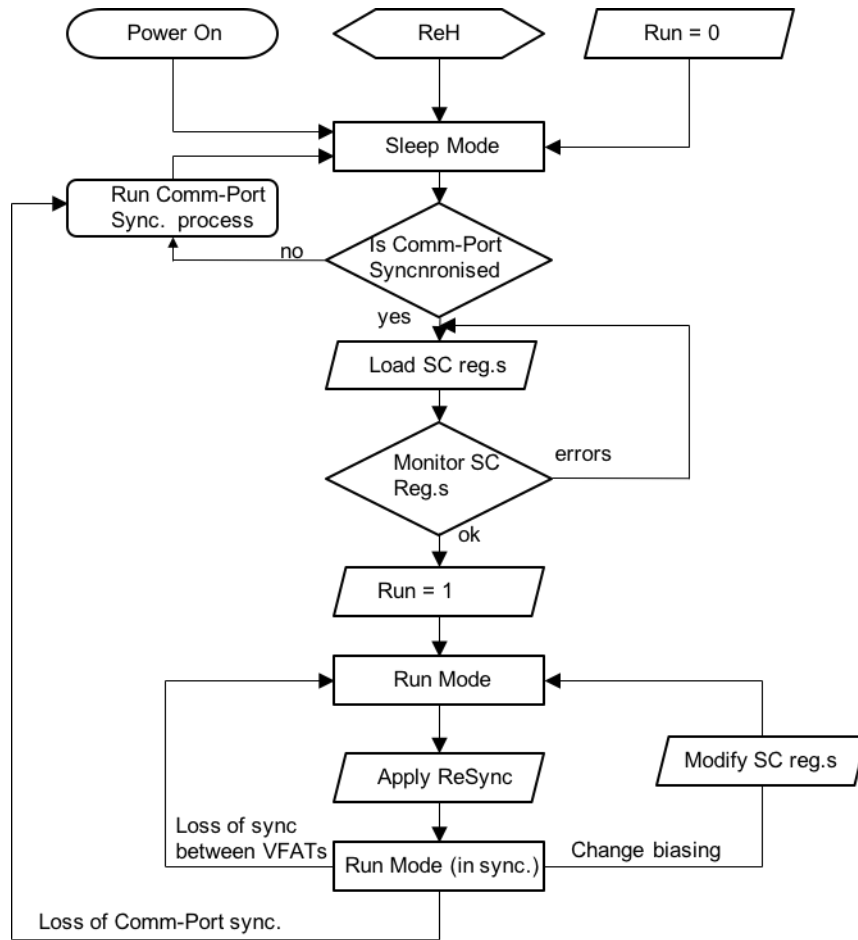
Figure 8: The VFAT3 Operational Flow

Reapplication of a ReSync signal may be required if synchronisation is lost. This can be detected by the monitoring of the data packets. It may also be necessary to change programmed Slow Control register values. It is possible to do this while running but it is advised not to do this during data taking. If register values have been changed then it is advised (although not always necessary) to reapply a ReSync signal.
Return to SLEEP mode is achieved by changing the SLEEP bit back to a logic 1.

1.7.1 Definition of Resets

There are a number of resets in VFAT3. These are summarized in Table 3.

Table 3: Table of the different types of RESETs in VFAT3.

Reset Name	Type	Internal Function
POR (power on reset) ReH Sleep = 1	Applying Power CMOS Pad SC CC command	SC reg.s set to default values, (SLEEP mode) Analog : nonfunctional minimum power consuming state Digital : SRAM and EC/BC counters reset and stopped
ReSync	CC Command	Realigns SRAM pointers, SRAM contents erased,
BC0	CC Command	Resets the BC (Bunch Crossing counter)

ECO	CC Command	Resets the EC (Event Counter)

2.   THE ANALOG FRONT END

2.1   General

The architecture of the front-end is shown in Figure 5 .

Architecture of the full-channel
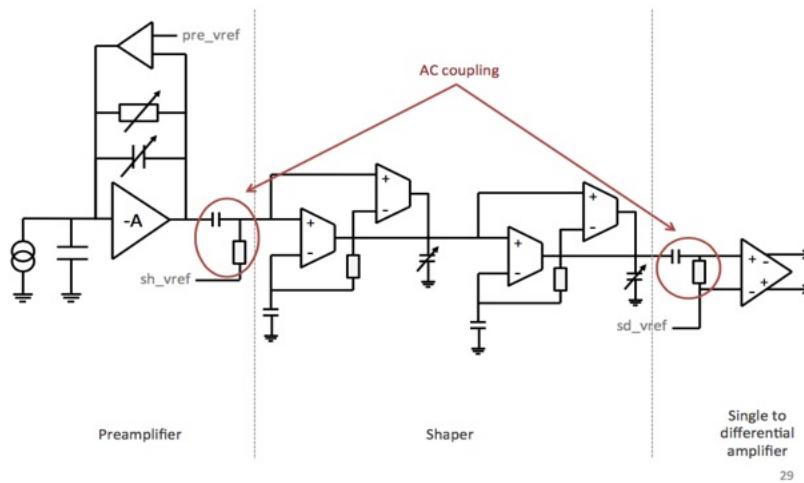
Figure 9: The Front-end architecture

The detector is dc connected to the preamplifier input. In this diagram the detector is modelled as a current source with a parallel capacitance. The front-end is then composed of preamplifier, shaper and single to differential stages, each of which are AC coupled to each other.

2.2   Front-end Simulation Results

The simulated pulse for the different shaping options are shown in Figure 6 and Figure 7 for "silicon" like delta input pulse and a "GEM" like current pulse. The waveforms are shown at the outputs of the preamplifier, shaper and single to differential stages.

Architecture of the full-channel

Preamplifier - Impulse response   Shaper - Impulse response   Single-to-differential – impulse response
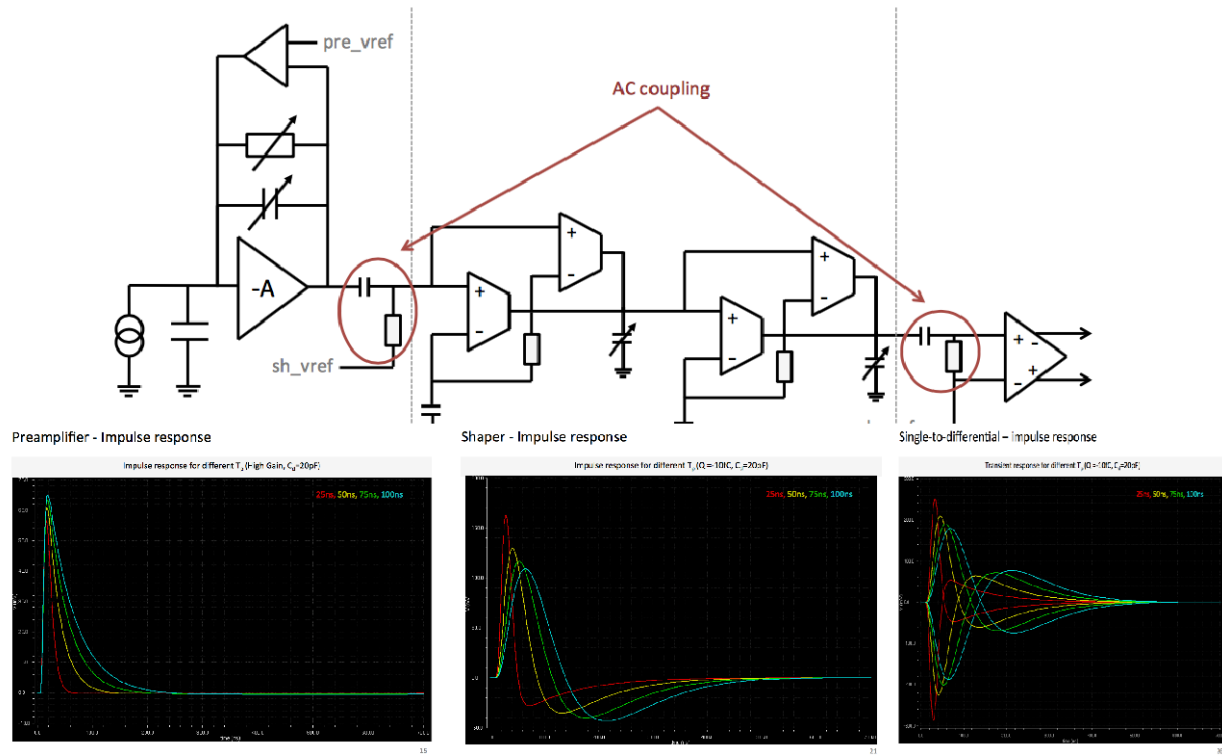
Figure 10: Simulated pulse shape responding to a delta pulse at the input.

Architecture of the full-channel
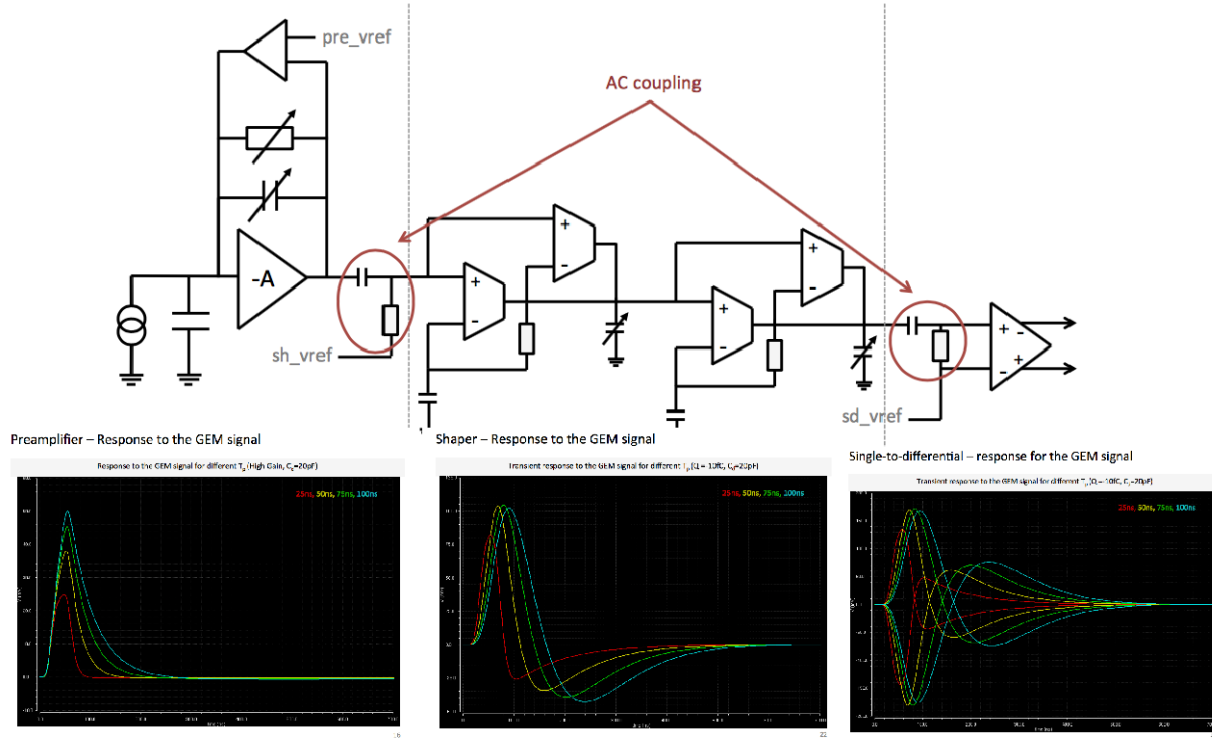
Figure 11: : Simulated pulse shape responding to a "GEM" like current pulse at the input.

2.3   Channel Input Protection

Two types of VFAT3 have been developed, VFAT3 and VFAT3prot (see Figure 34 for the differences in die sizes). The only difference between these two versions of VFAT3 is the type of input protection at the channel input pads.

Figure 8 shows the basic protection scheme as used in the VFAT3 version. It is based on standard ESD protection block made of two diodes, one to the supply bus and the other to the ground bus, as provided by the foundry I/O library.

The increased input protection circuit used in VFAT3prot version is shown in Figure 9. It includes a 7.5 Ω metal resistor which is inserted between the pad and four batches of anti-parallel larger diodes. The diodes have approximately a factor 12 increase in diode area with respect to the basic scheme.
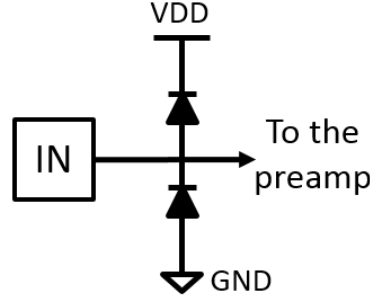
Figure 12: Basic channel input protection scheme, implemented in VFAT3.
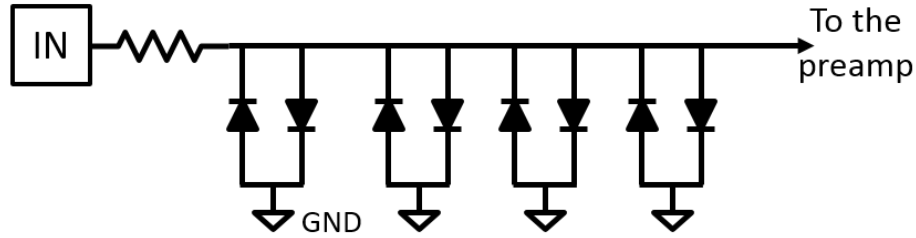
Figure 13: Additional channel input protection scheme, implemented on VFAT3prot.

3.   THE CFD

3.1   Architecture

A Constant fraction discrimination (CFD) is a technique to provide amplitude-independent information about arrival time of an event. The principle operation is based on detecting the zero-crossing of the bipolar pulse obtained by subtracting a fraction of the input unipolar signal to its delayed copy. It can be demonstrated that the bipolar pulse crosses the baseline at a fixed time with respect to the start of the pulse (Figure 13).

In VFAT3, the proposed implementation of CFD is based on a fully differential architecture for better noise rejection, shown in Figure 10. The differential input signals are sent to a passive shaping network that converts them into bipolar pulses with amplitude-independent zero-crossing time. The resulting bipolar pulses are then amplified by the post-amplifier that recovers the signal attenuation introduced by the shaping network and also applies a dynamic offset compensation.

Finally, the differential bipolar pulses are sent to the zero-crossing (ZCC) comparator that produces a digital pulse whenever its differential input crosses the baseline. The input signals are sent in parallel to an arming circuitry, in order to enable the CFD output only when the

input signal is larger than the programmed threshold provided by a global 8-bit digital-to-analog-converter (DAC). Moreover, both arming and ZCC comparators of each channel have their own 6-bit DAC to compensate mismatches among channels. Finally, a multiplexer allows the selection of the comparator output, according to bits SEL COMP MODE of the register GBL CFG CTR 3 as shown in Table 4. For instance, it is possible to bypass the CFD and use the arming comparator output without time-walk correction.
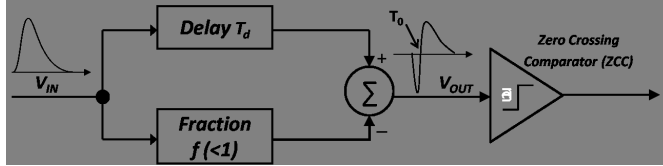
Figure 14: Scheme of CFD principle of operation
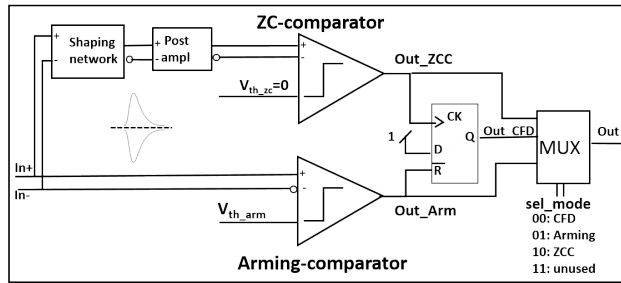
Figure 15: The CFD block diagram

Table 4: Selection of CFD output mode from GBL CFG CTR 3 register

Bits	Name	Description	State/Range	Initial value
1:0	SEL_COMP_MODE	Select CFD output mode	00: CFD	00
			01: Arming (leading edge)	
			10: ZCC	
			11: 0	

3.1.1 Shaping network

The shaping network is a fully differential cross-coupling passive network that implements and combines the delayed copy of the signal and its fraction to produce differential bipolar pulses with amplitude-independent zero-crossing time. It is based on a 4-stage R-C filter with programmable time constants (Fig.8), in order to fully exploit the CFD technique for each VFAT3 shaping time, using two bits of the GBL CFG CTR 3 register, as shown in Tab.5. In Fig.9 a typical transient response for 100 ns input signals with different amplitudes is shown. It can be noticed that the bipolar pulses cross in the same time t_0, which can be used as an amplitude-independent time tag.
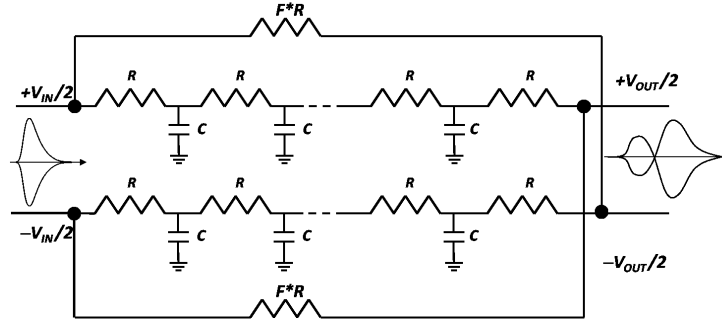
Figure 16: The shaping network with cross-coupling topology.

Table 5: Settings of shaping network parameters of GBL_CFG_CTR_3 register

Bits	Name	Description	State/Range	Initial value
9:6	PT	CFD time constant	0001: 25 ns	1111
			0011: 50 ns	
			0111: 75 ns	
			1111: 100 ns	

3.1.2 The comparators

The zero-crossing and arming comparators are based on the same high-gain differential amplifier followed by a chain of digital inverters, but they are different on the way the corresponding threshold is applied. In fact, in principle the ZCC comparator should have no threshold applied since it must detect the zero-crossing time but, in order to prevent it from firing on noise, a threshold is normally applied introducing an unbalancing between the two waveforms. As shown in Fig.10, when the outputs of the threshold circuit cross for the first time (phase (1)), the ZCC triggers and goes to "0". Once fired, the threshold is removed (phase (2)) and the next crossing (phase (3)) corresponds to the zero-crossing and ZCC goes to "1". Then, the threshold is again applied (phase (4)) until the next event. A farther protection preventing the ZCC comparator from firing on noise is implemented at its digital output, which is put in logical AND with the arming comparator output.

However, for debug and calibration purpose it is possible to bypass these two protections enabling the following two bits of the GBL CFG CTR 3 register:
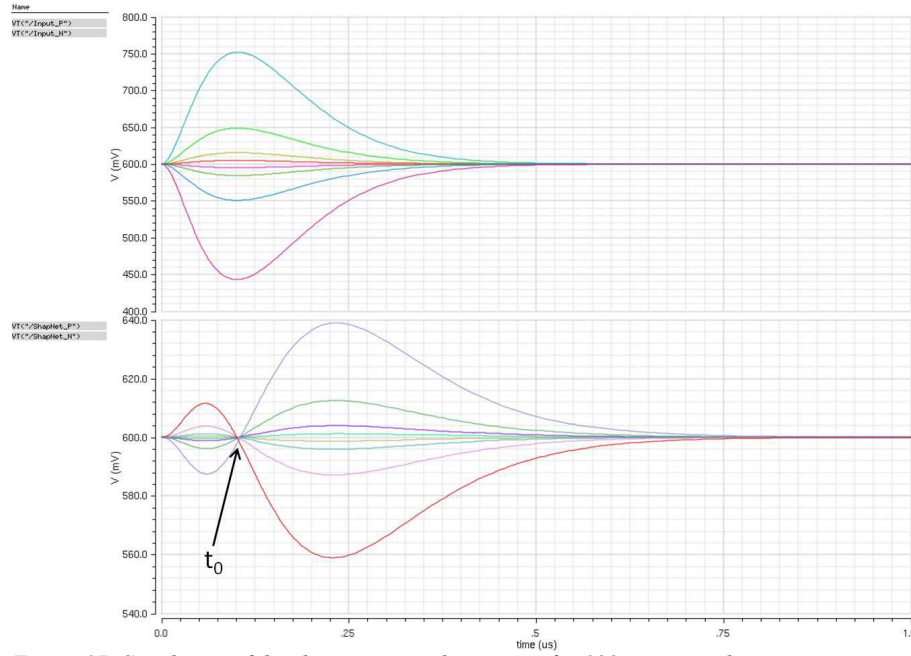
Figure 17: Simulation of the shaping network response for 100ns input pulses.

- FORCE TH: if enabled, it prevents the arming comparator from removing the ZCC threshold;
- FORCE EN ZCC: if enabled, the ZCC digital output is enabled regardless of the arming comparator.

3.1.3   Threshold settings

The global thresholds are provided by two 8-bit DACs, controlled by the register GBL CFG THR and summarized in Tab.6, while both arming and ZC comparators of each channel have their own 6-bit DAC to compensate mismatches among channels and controlled by the channel configuration register GBL CFG CH XXX, as in Tab.7

Bits	Name	Description	State/Range	Initial value
15:8	ZCC DAC	ZCC global threshold: nominal 0.5 mV/bit	0 - 0xFF	0x0b
7:0	ARM DAC	Arming global threshold: nominal 2 mV/bit	0 - 0xFF	0x20

Table 6: Global threshold settings from GBL_CFG_THR register

3.1.4   Hysteresis

The arming comparator has a programmable hysteresis, provided by a 6-bit DAC (nominal: 0.4 mV/bit) and controlled by the register GBL CFG HYS. For test purpose, it can also be disabled using the bit EN HYST of the register GBL CFG CTR 3.
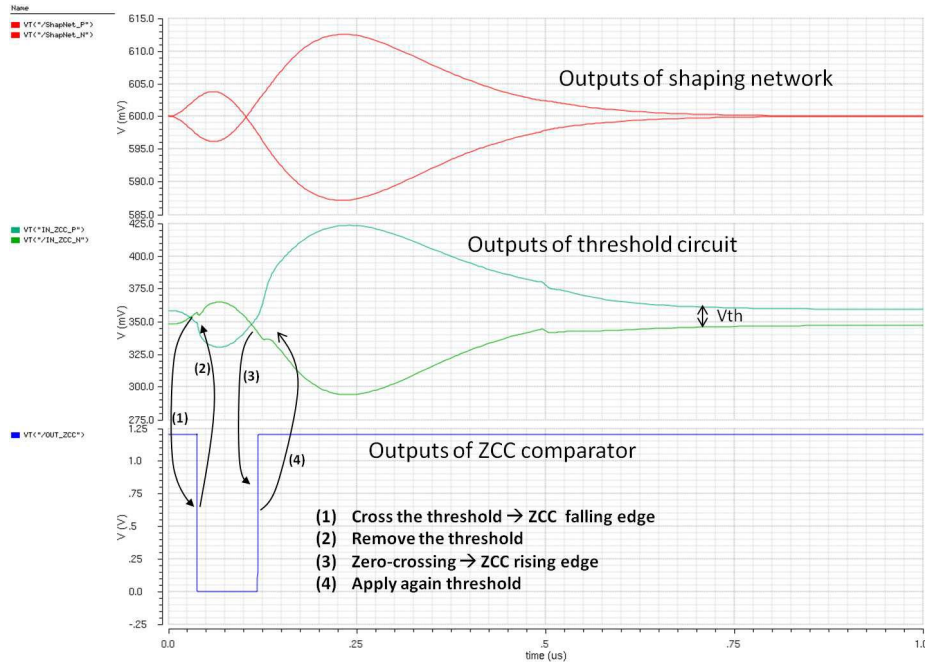
Figure 18: Timing diagram of the ZCC comparator

3.2 Layout

The layout of CFD is shown in Figure 13.
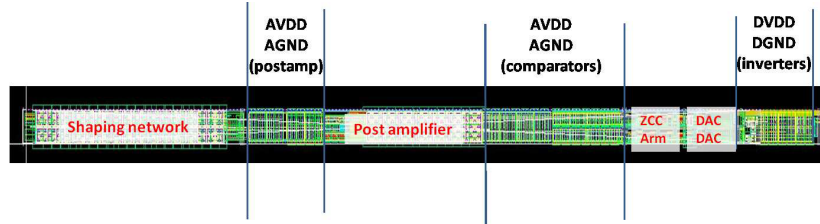
Figure 19: CFD Layout

The dimensions are: 60 μm x 1640 μm, including the power rails which are dimensioned to have a maximum voltage drop below 5 mV. The power domains are:
• AVDD CFD, AGND CFD: analog power supplies (I_{mean} _ 270 μA/channel), to be externally connected to Vdda and Gnda;
• DVDD CFD, DGND CFD: inverters power supplies (I_{mean} < 10 μA/chan, I_{peak} _ 300 μA/chan, to be externally connected to Vdda and Gnda or Vddd and Gndd ... yet to be understood;

• VDD CFD, VSS CFD: output flip-flop and mux, to be internally connected to digital Vddd and Gndd.

Table 7: Local thresholds settings from GBL CFG CH XXX register

Bits	Name	Description	State/Range	Initial value
13:7	zcc dac	ZCC local threshold: Bit 13 - polarity Bits 12:7 - amplitude (nominal 0.5 mV/bit)	0 - 0x7F	0x00
6:0	arm dac	Arming local threshold: Bit 6 - polarity Bits 5:0 - amplitude (nominal 0.5 mV/bit)	0 - 0x7F	0x00

3.3   Programmability and Bias Settings

The bias of CFD is provided by two 6-bit DACs controlled by the register GBL CFG BIAS 0, as described in Table 8, and can be used to adjust the bias in case of large process variations.

Table 8: CFD bias settings from GBL_CFG_THR register

Bits	Name	Description	State/Range	Initial value
11:6	BIAS DAC 2	CFD Bias2 current	0 - 0xFF	0x28
5:0	BIAS DAC 1	CFD Bias1 current	0 - 0xFF	0x28

3.4   Testability

As already mentioned in the front-end chapter, the 129th channels of VFAT3 is added for test purpose. As shown Figure 14, the two inputs and the output are directly accessible on I/O pads, allowing the injection of signals from external generators. The CFD output multiplexer allows to check the functionality of the three different operating modes (CFD, arming, ZCC) using one single output pad.
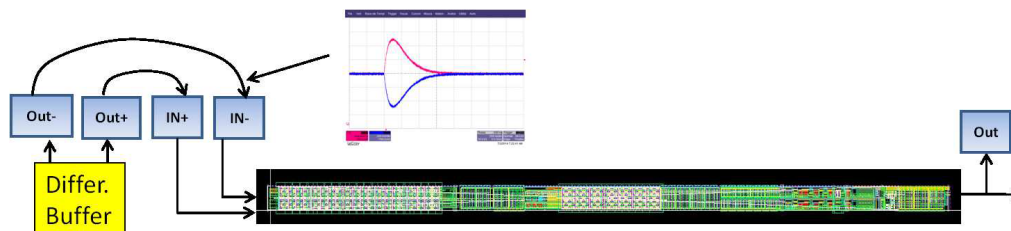
Figure 20: CFD test channel

4. CALIBRATION, BIAS & MONITORING (CBM)

CBM is the abbreviation for Calibration, Bias and Monitoring. The CBM unit is controlled by the Slow Control and provides the analog front-end and CFD biasing as well as the calibration functions.

4.1 The programmable Bias circuits

The analog biasing is programmable via 8 and 6 bit DACs in order to achieve optimal performance; taking into account both process variations and eventual degradation due to radiation damage. Hence the analog characteristics will change slightly over time and re-biasing from time to time may be necessary. For these reasons, programmable DACs were chosen to provide the necessary bias currents and voltages.
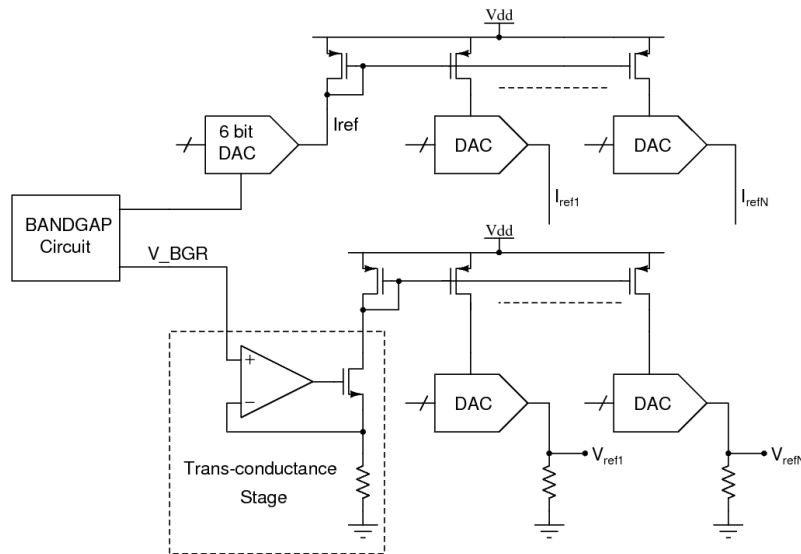
Figure 21: Architecture of the bias block.

The reference network has the structure shown in Figure 15. A single bandgap reference [1] provides a voltage and a current stable both in temperature and against the power supply voltage variations. A temperature simulation of the bandgap reference shows that in a range between 20 °C and 80 °C the maximum variation of both references is lower that 0:7% with respect to the nominal value at 27 °C.

4.1.1 The DACs (Programmable Bias Currents and Voltages)

VFAT3 contains 9x(6b) DACs & 8x(8b) DACs. In addition there are 129 local channel DACs for local threshold adjustment in each channel.

The DACs and their properties are shown in tables Table 9, Table 10 and Table 11.

Table 9 shows the current DACs which are used to set up current biasing and for generating voltage referencing and threshold. The bias name, DAC properties, associated programmable register and default/nominal values are given in the table. Note: the 3 biases listed with an * are used to set up voltages which are explained in Table 10. They are included in both tables as they can be monitored as either current or voltage.

Table 10 lists the programmable voltage references. Similarly to Table 9 the bias name, DAC properties, associated programmable register and default/nominal values are given in the table.

Table 9: DACs : Programmable Bias Currents

	Dac Type	LSB	Full Scale	Nominal Current	Default Word	Register	Address	Bits
Iref	DAC6	312,5 nA	20 uA	10 uA	32	GBL_CFG_CTR_5	0x00000086	5:0
CFD_Bias1	DAC6	500 nA	31.5 uA	20 uA	40	GBL_CFG_BIAS_0	0x0000008c	5:0
CFD_Bias2	DAC6	500 nA	31.5 uA	20 uA	40	GBL_CFG_BIAS_0	0x0000008c	11:6
CFD_Hyst*	DAC6	20 nA	1.26 uA	100 nA	5	GBL_CFG_HYS	0x00000088	5:0
CFD_ThArm*	DAC8	100 nA	25.5 uA	3.2 uA	32	GBL_CFG_THR	0x00000087	7:0
CFD_ThZCC*	DAC8	25 nA	6.735 nA	275 nA	11	GBL_CFG_THR	0x00000087	15:8
CFD_Iref_LocalDAC				25 nA				
Preamp_BiasInputTransistor	DAC8	1 uA	180 uA	150 uA	150	GBL_CFG_BIAS_1	0x0000008d	7:0
Preamp_BiasSource follower	DAC6	2uA	126 uA	26 uA	13	GBL_CFG_BIAS_1	0x0000008d	13:8
Preamp_BiasLeakage_comp	DAC6	1 nA	63 nA	25 nA	25	GBL_CFG_BIAS_2	0x0000008e	13:8
Shaper_BiasInputPair	DAC8	200 nA	51 uA	16 uA	80	GBL_CFG_BIAS_3	0x0000008f	7:0
Shaper_BiasFoldedCasc	DAC8	200 nA	51 uA	26 uA	130	GBL_CFG_BIAS_3	0x0000008f	15:8
SD_BiasInputPair	DAC8	200 nA	51 uA	28 uA	140	GBL_CFG_BIAS_4	0x00000090	7:0
SD_BiasFoldedCasc	DAC8	200 nA	51 uA	27 uA	135	GBL_CFG_BIAS_5	0x00000091	7:0
SD_BiasSource follower	DAC6	2uA	126 uA	30 uA	15	GBL_CFG_BIAS_5	0x00000091	13:8
SLVS_Ibias	DAC6	5 uA	315 uA	200 uA	40	GBL_CFG_BIAS_6	0x00000092	11:6

* These DACs control currents that are converted into voltages, please refer to table Voltage_Ref_Th

Note: Most settings are the same for VFAT3a and VFAT3b. However, there are 4 settings which are different between VFAT3a and VFAT3b due to a design update in the DACs to achieve the same nominal currents. Table 9 refers to the Default word settings for VFAT3b.

VFAT3a has 4 slightly different settings as follows:
****
Shaper_BiasInputPair = 150
Shaper_BiasFoldedCasc = 250

SD_BiasInputPair = 255
SD_BiasFoldedCasc = 255
****

Table 10: DACs: Programmable Bias Voltages

	Dac Type	LSB	Full Scale	Nominal Voltage	Default Word	Register	Address	Bits
Hyst_Vref	DAC6	0.4 mV	25 mV	2 mV	5	GBL_CFG_HYS	0x00000088	5:0
Vth_Arm	DAC8	2 mV	512 mV	64 mV	32	GBL_CFG_THR	0x00000087	7:0
Vth_ZCC	DAC8	500 uV	128 mV	5.5 mV	11	GBL_CFG_THR	0x00000087	15:8
Preamp_Vref	DAC8	5 mV	1 V	430 mV	86	GBL_CFG_BIAS_2	0x0000008e	7:0
SLVS_Vref	DAC6	10 mV	630 mV	400 mV	40	GBL_CFG_BIAS_6	0x00000092	5:0

An 8 bit DAC is also used for the magnitude of the calibration pulse whether in Voltage step mode or Current Pulse mode as indicated in Table 11.

Table 11: DACs : Calibration Settings

	CAL_MOD	Dac Type	CAL_FS	LSB	Full Scale	Register	Address	Bits
Voltage step	1			3mV	765 mV			
Current Pulse	2	DAC8	0	2.5 nA	637.5 nA	GBL_CFG_CAL_0	0x0000008a	9:2
			1	5 nA	1.275 uA			
			2	7.5 nA	1.9125 uA			
			3	10nA	2.5 uA			

4.1.2 *Monitoring the programmable Bias Currents and Voltages (The DACs)*

The internal DACs can be monitored to measure their characteristics. This is useful to precisely measure the calibration pulse charge and the current and voltage bias settings.

The monitoring system incorporates a multiplexing system to select which DAC to monitor and whether to monitor a current or a voltage. While in VFAT2 these currents or voltages were read by an off-chip ADC, VFAT3 has the ADC integrated within the chip.

The ADC measures voltages, hence the DAC currents need to be converted to voltages. This is done by routing the DAC current to an external "precision" resistor. Internally the ADC can then measure the resulting voltage. The voltage DACs can be monitored directly. The internal ADC is controlled and read via the VFAT3 Slow Control system.

Figure 16 shows the block diagram for the monitoring scheme. Please note that both these ADCs are internal but one uses an external reference. ADC0 uses an internal reference and ADC1 uses an external reference.
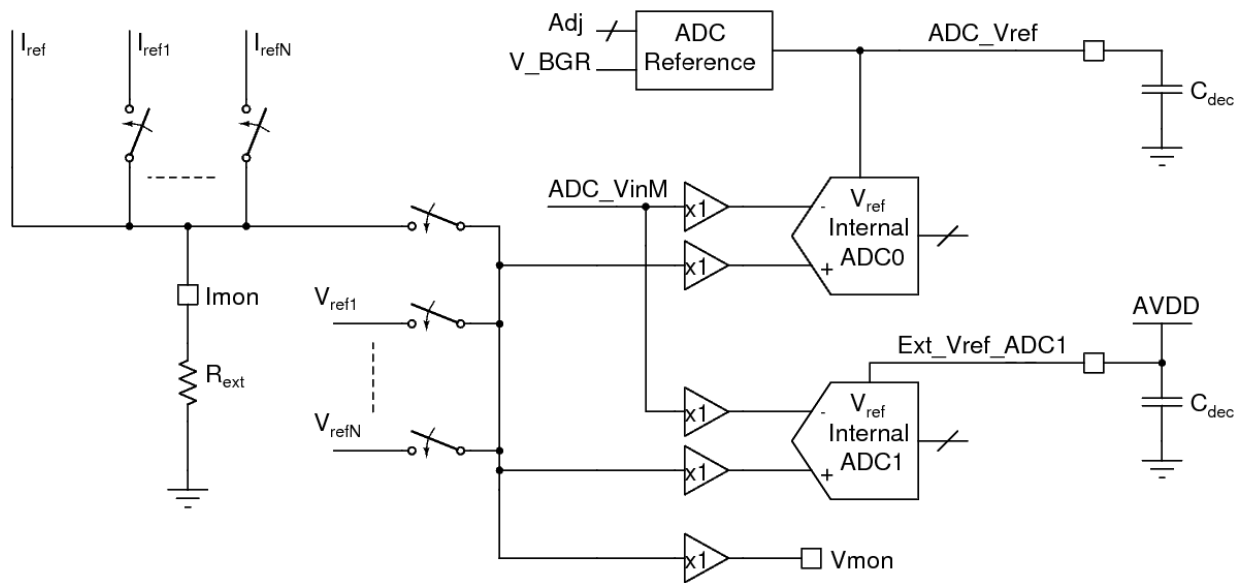
Figure 22: Monitoring circuit scheme.

The settings for monitoring the DACs voltages and currents plus calibration values are given in Table 12, Table 13 and Table 14.

Table 12: Monitoring the DAC Bias Currents

	GBL_CFG_CTR_4 Monitor_sel<5:0>	Scaling Factor	Current LSB	Voltage LSB 20kOhm	Measurement offset	Default value
Iref	0	0.5	156.25 nA	3.125 mV	0	5 uA
CFD_Bias1	10	1	500 nA	10 mV	Iref	20 uA
CFD_Bias2	11	1	500 nA	10 mV	Iref	20 uA
CFD_Hyst	12	1	100 nA	2 mV	Iref	500 nA
CFD_ThArm	14	1	100 nA	2 mV	Iref	3.2 uA
CFD_ThZCC	15	1	100 nA	2 mV	Iref	1.1 uA
CFD_Iref_LocalDAC	13	40			Iref	1 uA
Preamp_BiasInputTransistor	2	0.2	200 nA	4 mV	Iref	30 uA
Preamp_BiasSource follower	4	0.25	500 nA	10 mV	Iref	6.5 uA
Preamp_BiasLeakage_comp	3	100	100 nA	2 mV	Iref	2.5 uA
Shaper_BiasInputPair	6	1	200 nA	4 mV	Iref	16 uA
Shaper_BiasFoldedCasc	5	1	200 nA	4 mV	Iref	26 uA
SD_BiasInputPair	7	1	200 nA	4 mV	Iref	28 uA
SD_BiasFoldedCasc	8	1	200 nA	4 mV	Iref	27 uA
SD_BiasSource follower	9	0.25	500 nA	10 mV	Iref	7.5 uA
SLVS_Ibias	16	0.1	500 nA	10 mV	Iref	20 uA

Table 13: Monitoring the DAC Bias Voltages

	GBL_CFG_CTR_4 Monitor_sel<5:0>	Scaling Factor	Voltage LSB	Default Value
Vth_Arm	35	1	2 mV	64 mV
Vth_ZCC	36	4	2 mV	22 mV
Preamp_Vref	34	1	5 mV	430 mV
SLVS_Vref	41	1	10 mV	400 mV
ADC_Vref	39	1	50 mV	1 V
ADC_VinM	40	1		630 mV
V_Bandgap	32	1		330 mV
V_Tsensor_ext	38	1		
V_Tsensor_int	37	1		

Table 14: Monitoring the Calibration DAC values

	CAL_MOD	GBL_CFG_CTR_4 Monitor_sel<5:0>	Scaling Factor	CAL_FS	LSB	Voltage LSB 20kOhm	Measurement offset
Voltage step	1	33	1		3mV		0
Current Pulse	2	1	10	0	25 nA	500 uV	Iref
				1	50 nA	1 mV	Iref
				2	75 nA	1.5 mV	Iref
				3	100 nA	2 mV	Iref

4.2   Calibration Module

VFAT3 is equipped with a calibration circuit which can deliver internal pulses to each channel individually. This is an extremely useful feature for characterisation of the chip, production testing and for calibration purposes.

It is possible to choose between two different types of injection pulse. One is a voltage step pulse which is applied to a series capacitor generating a "delta" like pulse at the preamplifier input. This type of pulse is similar to that from a silicon detector. In this mode; the polarity, amplitude and phase of the pulse is programmable.

The second type of pulse is a current pulse applied directly to the preamplifier input. This type of pulse is more similar to a "GEM" like pulse. In this mode the magnitude of the current and the pulse duration are programmable.

Figure 17 shows the block diagram for the Calibration circuit. The blocks controlling the Voltage Pulse and the Current Pulse are shown as well as their connection to the channel preamplifiers via switches.
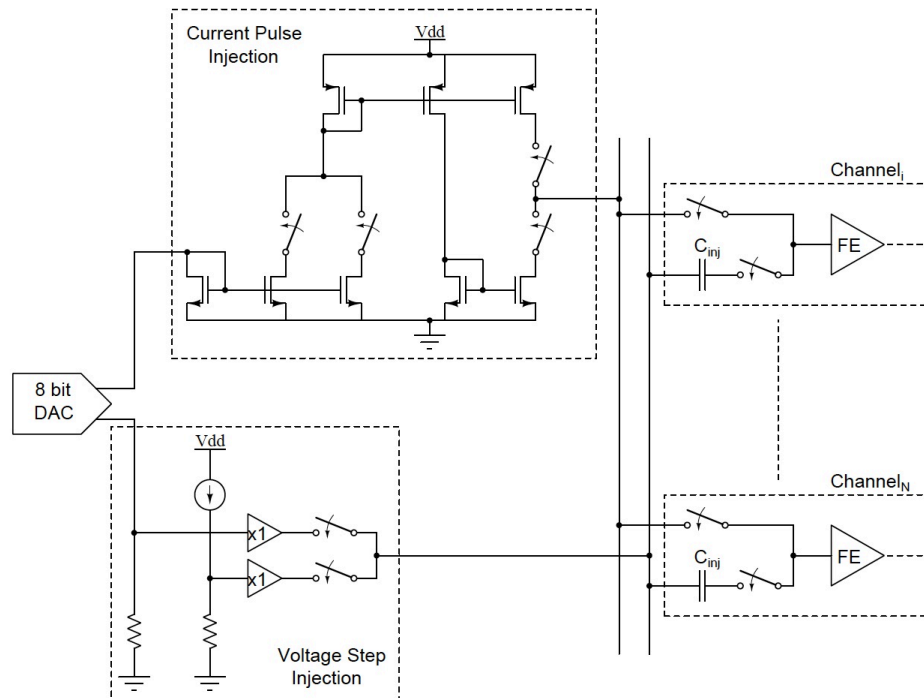
Figure 23: Architecture of the calibration circuit.

4.2.1   *Voltage step pulsing*

The principle of operation of injecting charge via a voltage step is shown in Figure 18. The step is produced between 2 dc voltages; namely V_{high} and V_{low}. V_{low} is a constant while V_{high} is programmable via an 8 bit DAC (CAL DAC in Table 30). The step is achieved by pre-charging with one dc value and switching to the other. The polarity setting will determine which voltage is the pre-charge and which is the value to switch to.

Voltage step – series capacitor

I_{ref} = 100 nA

I_{255} = 25.5 uA

$G_{buffers}$ ~ 0.8

R ~ 30 kΩ

$V_{MaxStep}$ ~ 600mV

8-bit Current DAC

V_{high}

T1

T2

100 fF

V_{high}

V_{low}

V_{low}

$V_{step} = V_{high} - V_{low}$

V_{high} and V_{low} can be read by monitoring ADC
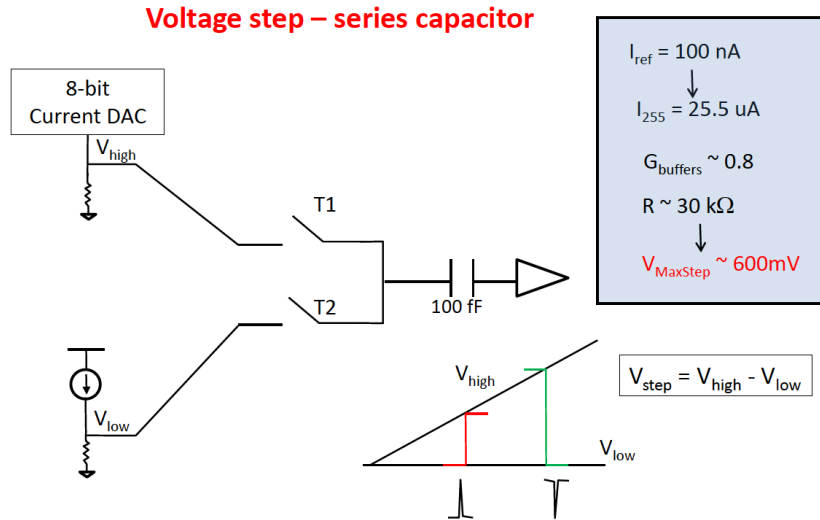
Figure 24: Voltage step generation - Principle of operation

Using the monitoring system, it is possible to scan the CAL DAC to measure V_{high} and V_{low} in dc. The difference between the two values multiplied by the 100 fF injection capacitor gives the injected charge (Q=CV). This can then be used as a look up table for choosing the charge to inject. Figure 19 plots the charge injected as a function of the CAL DAC value for both polarities. Note that in both cases they pass through 0 fC.

For monitoring V_{high}, and V_{low} , refer to both Table 25 & Table 30 to control the selection.
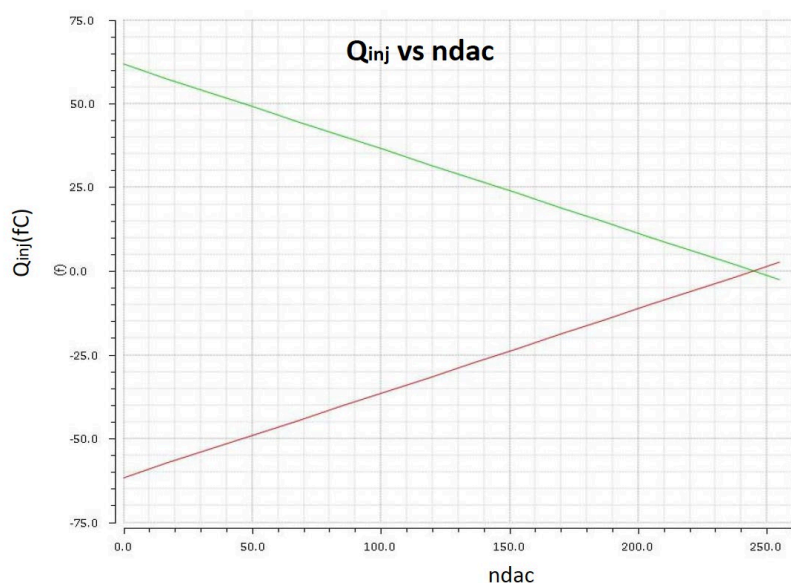
Figure 25: Simulated charge injected via the "Voltage Step". X axis is CAL DAC.

The selection of the channel is done through "cal" bit of each channel register (Table 20). Whilst it is possible to inject charge on multiple channels at once; it is not advised. This because the method of injecting charge relies on charge sharing, add more channels will reduce the accuracy of the injected charge.

The timing of the injection pulse is determined by the delivery of the CalPulse (Table 16). The phase can be adjusted in 8 steps of 3.125 ns using the CAL PHI bits of the calibration register 0 (Table 30), while its duration is controlled by the CAL DUR (Table 31) and must be set to its maximum value: 0x1ff.

4.2.2   Current pulsing

Figure 20 shows the principle of the current injection pulse. In this method a current pulse is applied directly to the input of an individual channel. To create the charge pulse, the dc current is switched between a sink and the preamp.

The magnitude of the current is determined by two different circuits: the DAC as used in the voltage step (CAL DAC in Table 30) and a scaling network controlled by the CAL_FS bits. Using the two CAL_FS bits the current pulse amplitude can be adjusted from 25% to 100% with a step of 25% (CAL_FS in Table 31).

In addition it is possible to program the duration of the pulse in terms of the 40MHz clock cycles. This is controlled by CAL DUR Table 31. It is recommended to set a value not larger than the peaking time: 25 ns, 50 ns, 75 ns or 100 ns.

The magnitudes of the injected charge are shown in Figure 21 for both polarities.

- A slow buffer gives a reference voltage ~ V_{in} to nodes A to decrease large transients
- Pulse width = 25 ns, 50 ns, 75 ns, 100 ns
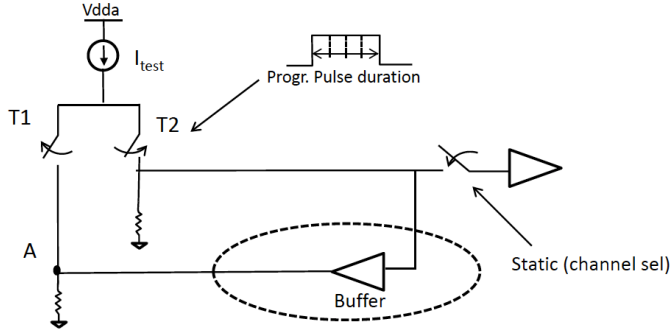
I_{test} **can be read by monitoring ADC**

Figure 26: Current Pulse Generation - Principle of operation
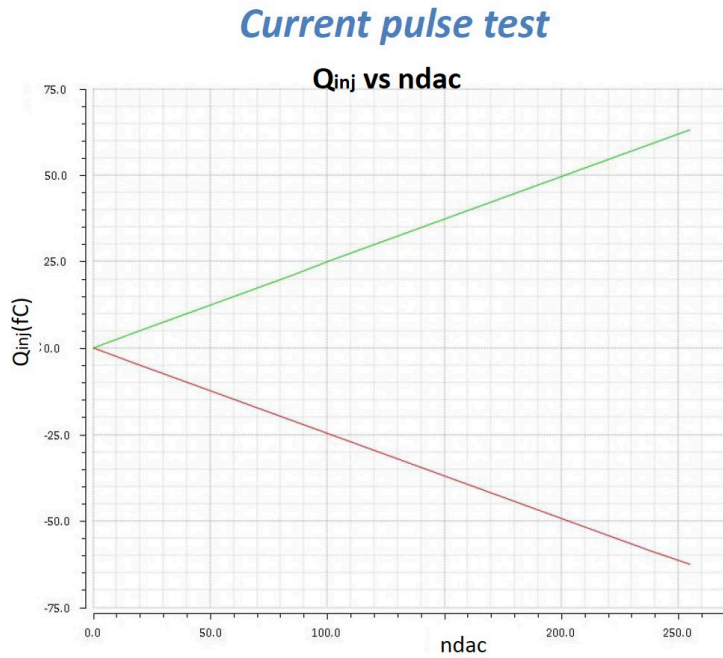
Figure 27: Simulated charge injected via the "Current Pulse" method. X axis is CAL DAC.

4.3 ADC

The ADC implemented for monitoring purposes is a 10 bit SAR ADC [1]. The SAR architecture was chosen because it has zero power consumption when not in use and can operate without a regular clock. The power consumption when in use is completely negligible. The ADC requires biasing and simply triggering to provide a sample.

There are 2 ADCs implemented within VFAT3; ADC0 and ADC1. ADC0 uses an internal reference derived from the bandgap while ADC1 has its reference tied to VDD using a dedicated pad. . The quality of the ADC bias affects the accuracy (effective number of bits) of the ADC. The environmental conditions may affect which one is the more accurate. Hence both were implemented in the chip. There are 2 "ADC READ" registers (one for each ADC), Table 44 & Table 45.

Figure 16 shows the 2 ADCs in the monitoring circuit scheme.

Selection of the dc value to sample and monitor is done as explained in section 4.1.2 .

The trigger to start an ADC sample is provided by an internal state machine in the slow control logic. The state machine to read the ADC is activated when one of the ADC READ registers is accessed for "read".

A closer look at the circuit blocks surrounding the ADC is shown in Figure 22 and the ADC transfer characteristic is show in Figure 23 .
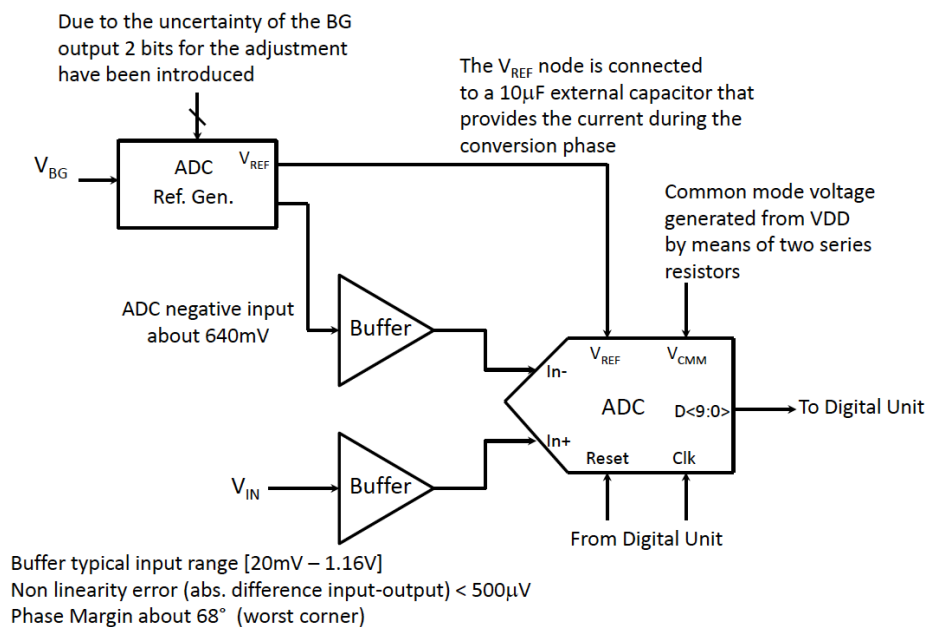
Figure 28: The ADC circuitry
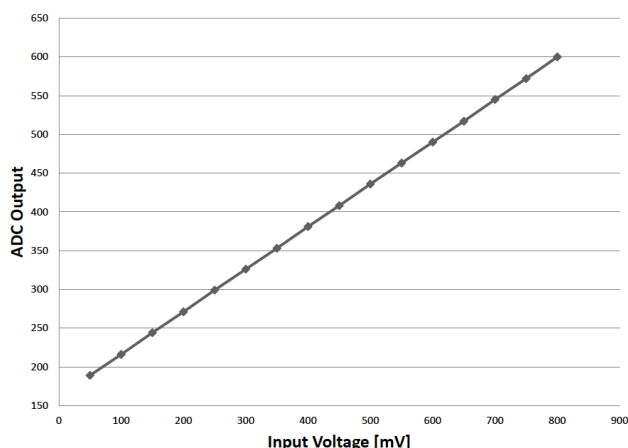
Each point is obtained after 3 consecutive conversions

Figure 29: The ADC transfer function.

4.4   Temperature sensor

The architecture of the temperature sensor, shown in Figure 24, is made by two main sections: the temperature sensitive device and the output stage.
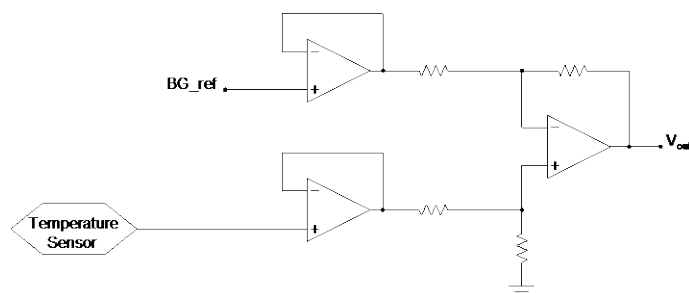
Figure 30: The architecture of the temperature sensor.

The first one is based on the standard PTAT architecture (Positive To Absolute Temperature) where the two diode connected BJTs have been replaced by NMOSTs. These two transistors, that are the temperature sensitive devices, are high VTH NMOS biased in weak inversion. They have been designed with a high aspect ratio in order to have a good linear response over a wide range of temperature and to improve their radiation hardness. The output stage, composed by the three OpAmps in fig. 19, amplifies and shifts the output voltage of the PTAT stage to increase the sensitivity and to keep the output swing in the power supply range.

The reference voltage (BG PV in fig. 19) used to shift the output characteristic is provided by the internal bandgap circuit (about 300mV).

The power supply of all components is provided by a dedicated pad, so that the circuit can be independently switched on or off from the entire chip (it is useful in case of a malfunctioning of the sensor).

The sensor specifications are reported in Table 15.

31

Table 15: Temperature sensor simulation

Sensitivity	3.78mV/ ℃
Temperature Range	−100∘C ÷ +100∘C
Output dynamic range	140mV ÷ 900mV

Figure 31 shows nominal simulation of the sensor output characteristic with the relative linear fitting is shown.
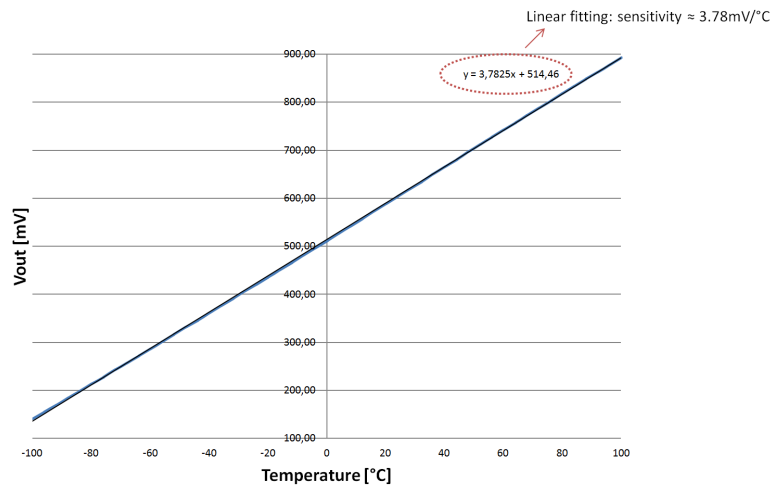
Figure 31: Temperature sensor characteristic with linear fit

The internal temperature sensor is read through the slow control system. An example of a measured result is shown in Figure 32 .
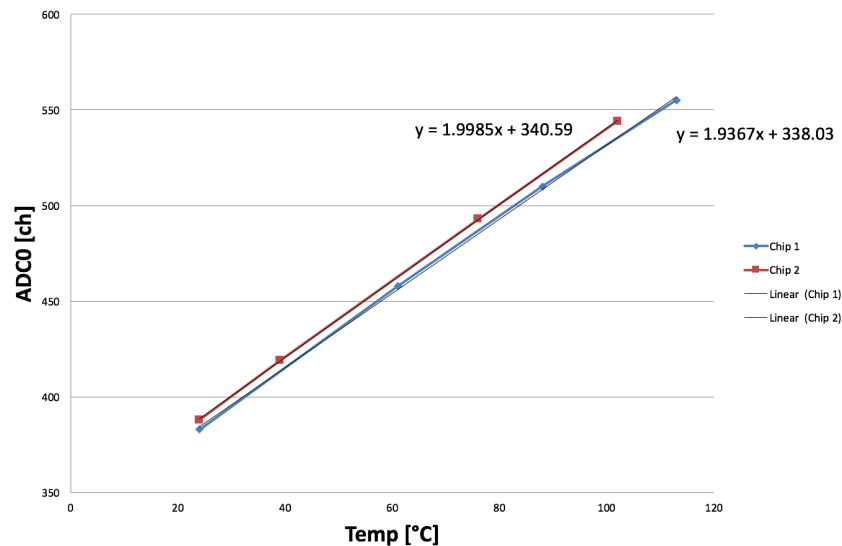
Figure 32: An example of reading the internal temperature sensor. In this case using the internal ADC0. The results from two chips are displayed showing a dc offset between the two.

In this case the internal ADC0 was used to measure the voltage "V Tsens Int" . The ADC LSB = 1.95mV giving a measured sensitivity of the temperature sensor of 3.83mV/ºC. Once calibrated, the error of the measurement is approx.. +- 3 ºC.

5.   COMMUNICATION WITH VFAT3

Communication with VFAT3 is through the Comm-Port and is designed such that VFAT3 is compatible with the GBT running with an e-link of 320MHz. This means that 1 GBT can communicate with 10 VFAT3 chips.

The e-link itself is composed of 3 differential SLVS pairs running at 320MHz. The 3 pairs are "Clock, DataIn and DataOut when seen from the VFAT3 side.

5.1   The Comm-Port
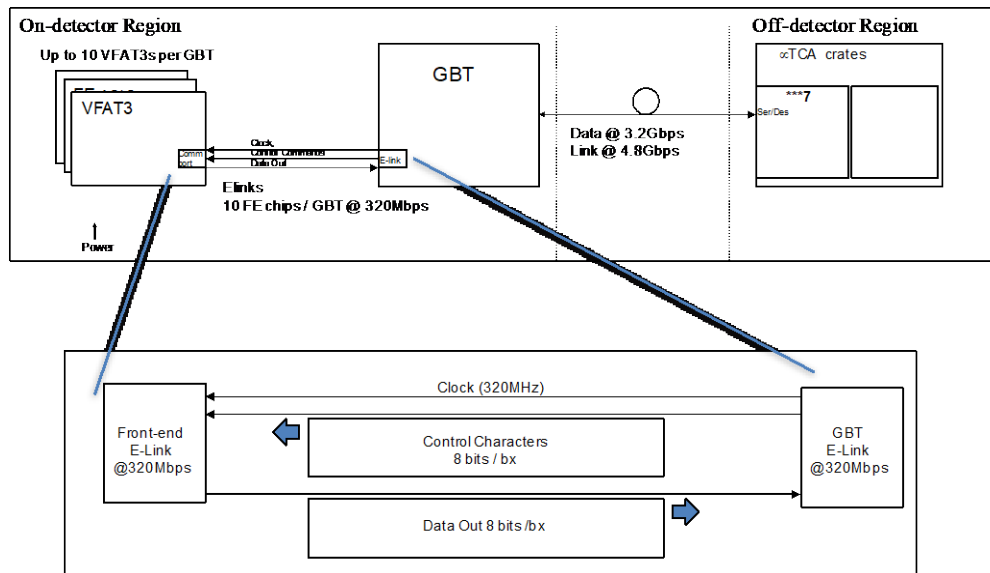
Figure 33: Communication with the GBT

These pairs have the following functions:

Clock: Apply a 320MHz continuous clock. The internal 40MHz sampling clock is derived from this 320MHz clock hence precise control of signal quality and jitter is important.

DataIn: The control of VFAT3 is achieved through Control Commands on this SLVS pair. The same port is used for Slow Control communication as well the delivery of "fast" synchronous control commands.

DataOut: The DataOut is used for the transmission of data, chip status and slow control return data.

A block diagram of the Comm-Port interface is shown in Figure 27 .
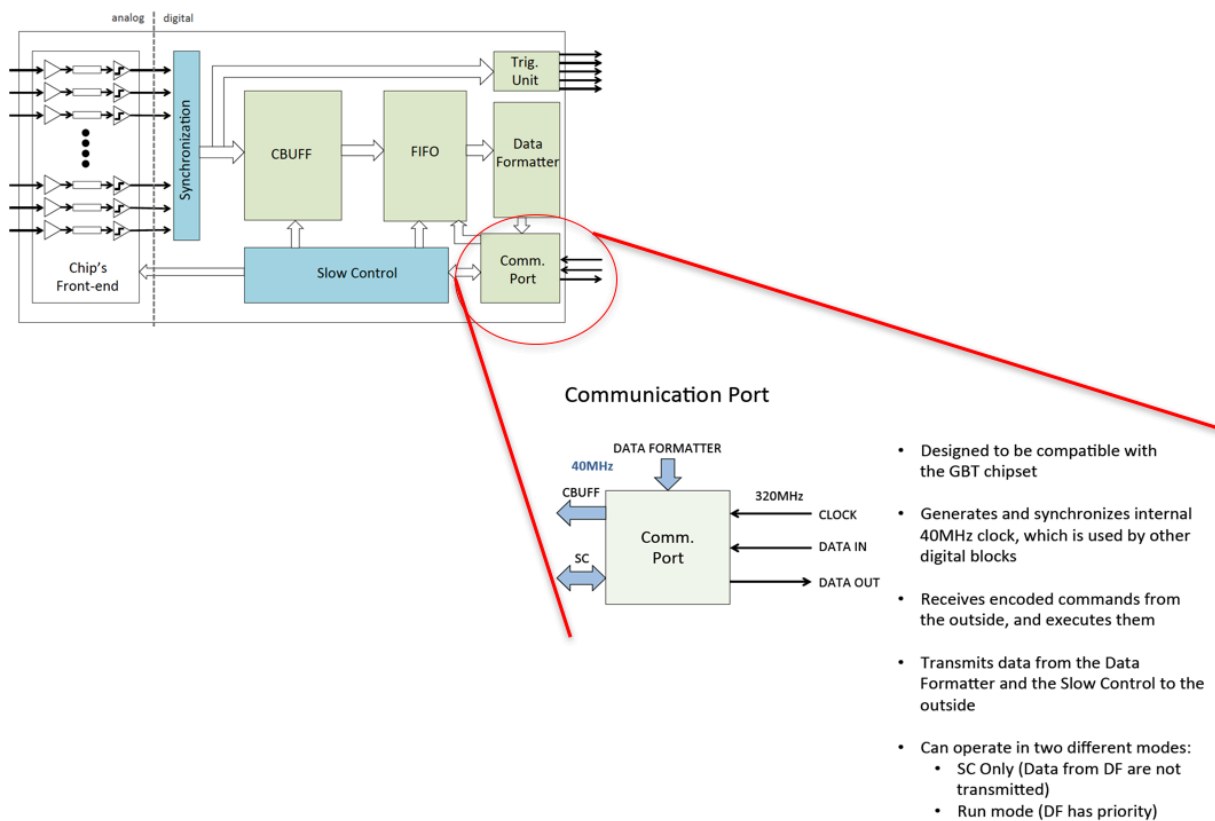
Figure 34: The CommPort

The Comm-port is used to send and receive both Slow Control information, Control and Status commands and Data through a single port. It receives Command characters and sends the relevant commands to the internal Slow Control system or the Control logic of the memories. It also receives information from the Slow Control system and the Data Formatter to send information back to the GBT.

5.2 VFAT3 Control Characters (DataIn)

Table 16: The VFAT3 Command Characters for "DataIn"

Name	4-bit word	8-bit representation	Command
A	0000	00000000	-
B	0001	00001111	EC0
C	0010	00110011	BC0
D	0011	00111100	CalPulse
E	0100	01010101	ReSync
F	0101	01011010	SC Only
G	0110	01100110	Run Mode
H	0111	01101001	LV1A
I	1000	10010110	SC0
J	1001	10011001	SC1
K	1010	10100101	ReSC
L	1011	10101010	LV1A+EC0
M	1100	11000011	LV1A+BC0
N	1101	11001100	LV1A+EC0+BC0
O	1110	11110000	EC0 + BC0
P	1111	11111111	-
CC-A		00010111	Synchronization
CC-B		11101000	Verification of Sync

The list of Control Characters that the Comm-port responds to is shown in Table 16. There are 2 phase insensitive characters (CC-A and CC-B).
Phase synchronisation of the internal 40MHz sampling clock is achieved by sending 3 times the CC-A character as a 24 bit code. The 40MHz internal clock phase will then align to the CC-A 8 bit word.
The CC-B command is used to check the phase.

It is required to synchronise the Comm-port before sending any of the other commands as all the other commands are not phase insensitive.

There are a number of fast commands such as EC0 and BC0 for resetting the time tag counters. CalPulse to initiate a calibration pulse, ReSynch to realign the memory pointer and LV1A to send a trigger. There is also some code that send multiple commands simultaneously.

Accessing the Slow Control unit is done by sending SC0 and SC1 characters that send a logic "0" or "1" to the Slow Control" unit. Since these are 8 bit codes running at 320MHz, it follows that the access to the Slow Control is done at 40MHz.

Since the Comm-Port is used for both data and slow control, it is necessary that a priority system is set-up. The Comm-Port takes care of this by making the Data have priority over the slow control functions. However, it is possible to force the Comm-Port to ignore Data and work in Slow Control Only mode by sending and "SC Only" command. Return to the default Data Priority mode is achieved by sending a "Run Mode" command.

5.3   VFAT3 Characters (DataOut)

The DataOut pair from VFAT3 is continually active sending F1/F2 characters in a toggling state during "Idle" periods.

In Slow Control communication the returning characters are SC0 and SC1 to indicate slow control logic "0" and "1" respectively.

The SyncAck and SyncVerifAck codes are returned after synchronisation (via 3xCC-A) or a request for verification of synchronisation.

These codes are shown in Table 17.

Table 17: The VFAT3 Codes on DataOut

Name	8-bit representation
F1	01111110
F2	10000001
SC0	10010110
SC1	10011001
SyncAck	00111010
SyncVerifAck	11111110

The data packets from VFAT3 are also transmitted on the DataOut pair. Details of the Data Packet format is explained in Section 6 .

6. DATA FORMATS

The data packets from VFAT3 have the general form :

- Header
- Time Tags
- Data Field
- CRC

Whilst this is the general form, the data packet contains a very high level of flexibility and programmability. This allows reducing the data packet size to the minimum optimal size depending on the application, particularly useful for high rate environments. The register for programming the Data Packet contents is Table 22: GBL CFG CTR 1: Data Packet Settings .

Figure 28 and Figure 29 show the programmable options for two main types of data packet. These are Lossless and SPZS. Selection of the Data Type is done by programming the "DT" value.

6.1 Data Packet generalities

The time tags are the "Bunch counter" (BC) and the "Event Counter" (EC). The BC is incremented for every 40MHz internal clock and the EC is incremented for every LV1A received by VFAT3. In some cases it may be desirable to suppress one of these time tags which can be done by the "TT" setting. In addition the bit size of the time tag is programmable via "BCb" and "ECb".

An option exists for suppressing the entire data field if there are no "hits" present. The "SZD" (Suppress Zero Data) parameter controls this. Note that applying this will mean that the data field length becomes data dependent.

The "Header" changes to indicate that the data field has been zero suppressed, indicated by Header I and Header II. There are 2 other versions of the Header which are shown in Figure 28 and Figure 29 as Header IW and Header IIW. The "W" versions appear when the data FIFO (SRAM2) becomes half full and can be used as a trigger throttle.

It is also possible to suppress the entire data packet contents in the absence of a hit. This is controlled by SZP (Suppress Zero Packet). In this case, if there are no "hits" for a given trigger, the only information sent is the Header.

The CRC is type 16-bit CCITT, the polynomial = 1021 HEX and the initial value = FFFF.

6.2   The Lossless data packet

Figure 28 shows the lossless data packet structure. The lossless data field contains 128 bits for the 128 channels of VFAT3. A "0" represents a channel without a "hit" and a "1" represents a channel with a "hit". This is similar to the data field in VFAT2.

Lossless Data Packets					
Registers			**Data Packet**	**No. Bits**	**Comment**
DT	SZP	SZD			

0	0	0

Data Packet	No. Bits	Comment
Header I / Header IW	8	**Basic data packet**
EC+BC / EC / BC	8 - 48	Size depends on TT, Ecb, BCb
Data	128	
CRC	16	

0	0	1

Data Packet	No. Bits	Comment
Header I / Header IW	8	**Basic data packet**
EC+BC / EC / BC	8 - 48	Size depends on TT, Ecb, BCb
Data	128	
CRC	16	
Header II / Header IIW	8	**Zero Suppressed**
EC+BC / EC / BC	8 - 48	Size depends on Ecb
CRC	16	

0	1	x

Data Packet	No. Bits	Comment
Header I / Header IW	8	**Basic data packet**
EC+BC / EC / BC	8 - 48	Size depends on TT, Ecb, BCb
Data	128	
CRC	16	
Header II / Header IIW	8	**Zero Suppressed**

Header	8-bit representation
Header I	00011110
Header IW	01011110
Header II	00011010
Header IIW	01010110

Figure 35: The Lossless Data Packets

6.3   The SPZS data packet

In this data packet the data field changes in size depending on the number of channels hit for a given trigger.

Relevant registers		

SPZS (Sequential Partial Zero Suppression) Data Packets					

ECb table:

ECb	Size(EC)	
00	8	*default*
01	16	
10	24	
11	(8)	

BCb table:

BCb	Size(BC)	
0	16	*default*
1	24	

TT table:

TT	EC+BC / EC / BC	
00	EC + BC	*default*
01	EC	
10	BC	
11	(EC + BC)	

Registers / Data Packet table:

DT	SZP	SZD		Data Packet	No. Bits	Comment
1	0	0		Header I / Header IW	8	*Basic SPZS data packet*
				EC+BC / EC / BC	8 - 48	Size depends on *Partitions/P16*
				Data	16 - 144	
				CRC	16	
1	0	1		Header I / Header IW	8	*Basic SPZS data packet*
				EC+BC / EC / BC	8 - 48	Size depends on *TT, Ecb, BCb*
				Data	16 - 144	Size depends on *Partitions/P16*
				CRC	16	
				Header II / Header IIW	8	*Zero Suppressed*
				EC+BC / EC / BC	8 - 48	Size depends on *Ecb*
				CRC	16	
1	1	x		Header I / Header IW	8	*Basic SPZS data packet*
				EC+BC / EC / BC	8 - 48	Size depends on *TT, Ecb, BCb*
				Data	16 - 144	Size depends on *Partitions/P16*
				CRC	16	
				Header II / Header IIW	8	*Zero Suppressed*

Partitions table:

Partitions	No. Partitions
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14
1110	15
1111	16

P16 table:

P16	Comment	
0	Send numbers of partitions accodring to **Partitions** register	*default*
1	Send only high level information (16bit)	

Figure 36: The SPZS Data Packet

Figure 30 shows the SPZS data field sequence. The 128 channels are divided into 16 partitions, each partition containing 8 channels. The sequence begins with 16 bits indicating which partitions contain hits, this is then followed by the contents of each partition.

Partition List	Channel Correspondence
p15	<127:120>
p14	<119:112>
p13	<111:104>
p12	<103:96>
p11	<95:88>
p10	<87:80>
p9	<79:72>
p8	<71:64>
p7	<63:56>
p6	<55:48>
p5	<47:40>
p4	<39:32>
p3	<31:24>
p2	<23:16>
p1	<15:8>
p0	<7:0>

Channel List
of 1st partition
in the partition
list. 8b
<msb:lsb>

Channel List
of 2nd partition
in the partition
list. 8b
<msb:lsb>

etc

Figure 37: The SPZS data field sequence.

7. THE SLOW CONTROL

7.1 Hardware protocol

The bit stream containing the command to the slow control (SC) block is multiplexed inside the main bit stream received by the VFAT3 chip at 320 Mbps through the Comm-port (CP). Due to encoding and multiplexing, the rate of bits reaching the SC is limited to 40 Mbps in both the transmission directions and the flow can be suspended by high priority data or control signals. The signals connecting the SC block to the communication block, synchronous to 40 MHz, are explained in detail in Table 18.

Table 18: Definition of the communication signals between the Slow Control block and the Comm-port

Name	Direction	Description
RXD	CP $\Rightarrow$ SC	Data from the Comm-port to the Slow Control
RX EN	CP $\Rightarrow$ SC	High : data on the RXD line is valid and can be processed, else it is ignored.
TXD	SC $\Rightarrow$ CP	Data from the SC to the Comm-port.
TX ACK	CP $\Rightarrow$ SC	High: data on the TXD line is accepted from the Comm-port and the Slow Control can put the next bit on the TXD line on the next clock cycle, else the

		data is hold while the TX ACK is low.
TX DTS	SC ⇒CP	High: The Slow Control has data to send in response to a received request. As soon as it can, the Comm-port will put high the TX ACK line to start the data transmission.

7.2   Line Encoding

The bit stream is encoded following a subset of the HDLC standard, implemented as in the RFC1662 "PPP in HDLC-like Framing". The structure of the HDLC frame, as implemented in VFAT3 is shown in the Table 19. The bits are sent LSB first.

Table 19: HDLC frame structure

8	8	8	variable	16	8
FS	Address	Control	Data	FCS	FS

FS: Frame separator. A sequence of 01111110. To make it an unique sequence in the bit stream, the bit-stuffing technique is applied to the frame content.

Address: Address of peripheral station. When a primary station sends a frame, the address field contains the receiver identity, that will be compared with the local station address and the broadcast address (0xff). Frames with unrecognized Addresses are discarded. When VFAT3 sends a frame, the address field contains the sender identity, derived from the configuration pins state (HDLC ADDRESS).

Control: Following the RFC1662, the Control field is a single octet, which contains the binary sequence 00000011 (hexadecimal 0x03), the Unnumbered Information (UI) command with the Poll/Final (P/F) bit set to zero.

Data: The payload, i.e. the IPbus commands or responses.

FCS: The Frame Check Sequence field, 16 bits (two octets). The FCS is transmitted least significant octet first, which contains the coefficient of the highest term. Contains CRC check evaluated using the CRC-16-CCIT standard, described by the polynomial:
FCS [16 bits] = $X^{16} + X^{12} + X^5 + 1$
Details on the CRC evaluation can be found in the RFC1662 – Appendix C.

7.3   Bit Stuffing

If the flag bit sequence exists in the frame fields but FS, bit stuffing is used. If the sending station detects five consecutive 1s in other field, it stuffs (inserts) an extra 0 after the fifth 1. Whenever a 0 follows five consecutive 1 s, the receiver assumes the 0 was stuffed and remove it. Note that the flag field itself is not subject to bit stuffing and it is the only place where the flag pattern can appear.

data
0 0 1 1 1 1 1 1 1 0 0

transmitted data
0 0 1 1 1 1 1 0 1 1 0 0

first bit   "stuff" 0 bit after the fifth 1

stuffed bit

(a) More than five consecutive 1s

data
0 1 1 1 1 1 0 1 1 0 0

transmitted data
0 1 1 1 1 1 0 0 1 1 0 0

first bit   "stuff" 0 bit after the fifth 1

stuffed bit

(b) Five consecutive 1s
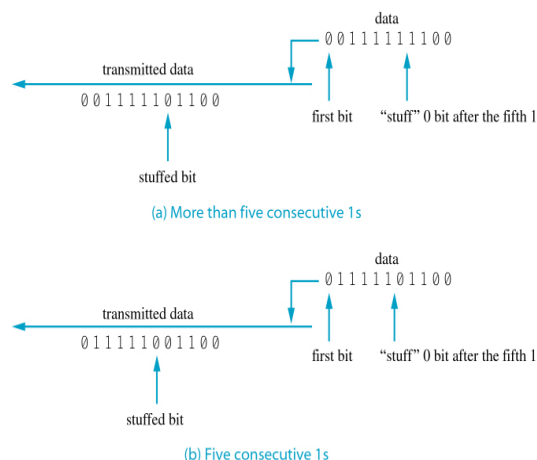
Figure 38: Bit Stuffing

7.4　E-Fuse (Chip ID)

VFAT3 contains a 32 bit E-Fuse. The purpose of the E-Fuse is to allow the programming of a unique code for use as a chip ID. The programming should be done during the production test phase and can only be done once. The reading is done via the slow control and can be read without limit. It is therefore useful to link this code with a database for storing constants, calibration information, mapping on the detector etc.

7.4.1　E-Fuse - Programming

Programming of the E-Fuse is achieved by controlling the voltage on pin labelled "VDD_EFUSE" using the eFuse HW prog register (Table 43) and simultaneously controlling the voltage of VDD_IO.

The normal voltage for VDD_EFUSE and VDD_IO is 1.2V. However, this needs to be raised to 2.5V during the programming phase of the E-fuse. It is important to note that all other VDD power supplies for the chip remain at 1.2V and that the 1.2V supplies should be applied and stable before raising the VDD_EFUSE and VDD_IO to 2.5V.

Each bit of the 32 bit code is programmed separately. The address of the bit to be programmed is set in the HW prog register (Table 43), "PRG BIT ADD". The time period for which the programming of each bit performed is an important parameter. The minimum time permitted is 10us and the maximum is 30us. 20us is hence a good number to use and can be set in the same register ("PRG TIME").

Each "write" command to this register initiates the writing of a logic "1" to the bit indicated by the "PRG BIT ADD". The actual burning time is defined by the "PRG TIME". Multiple bits may be written to by queuing up successive "Write" commands within one HDLC packet.

Hence the procedure to write to the E-Fuse is the following:

Unwritten bit = 0
Written bit = 1

1. Power on the chip and synchronise the link.
2. Raise the VDD_EFUSE & VDD_IO to 2.5V.
3. Write to the HW Prog Register (prg_time, prg_bit_add)
4. Write to the HW Prog Register (prg_time, next prg_bit_add)
5. Write to the HW Prog Register (prg_time, next prg_bit_add)
6. Write to the HW Prog Register (prg_time, next prg_bit_add)
7. Etc.
8. Return VDD_EFUSE and VDD_IO to 1.2V for normal operation.

The E-FUSE can only be written to once in the life time of the chip. Since this will be a "Chip ID", great care needs to be taken to ensure multiple chips are not written to the same code.

7.4.2   E-Fuse (Chip ID) - Reading

The output of the E-fuse is stored in a dedicated Chip ID register which has the address as given in Table 42 . The reading of the Chip ID is therefore the simple task of reading this register.

7.5 Registers

All control and status registers are mapped onto a local Wishbone bus. The ADc and Hardware ID are also connected to the same bus. The Wishbone bus can be controlled by two masters; the IPbus transactor and an auxiliary SPI master. The latter connected to a set of external pins.

The list of registers follows. The field **ID of register** is the symbolic name assigned in the file regmap.inc. The field **typedef** is the name of the System Verilog structure describing its content.

Table 20: Channel Control Register, 1 per channel

ID of register	GBL CFG CH 0 to GBL CFG CH 129	Size	16 bits
Address	0x00000000 to 0x00000080	Read/Write	Read/Write
typedef	cfg channel t		

Bits	Name	sub bits	Description	State/Range	Sleep
15	cal		Enable the calibration pulse to the channel input	0 = disable 1 = enable	0
14	mask		Mask the channel output for trigger and readout	0 = unmasked 1 = masked	0
13:7	zcc dac		Zero Crossing Comparator Timing optimisation	0 x00 – 0x7f	0x0
		13 12:7	correction polarity correction amplitude	0=Pos, 1=Neg 0=No correction LSB=0.5 mV	
6:0	arm dac		Arming Comparator Threshold trimming	0 x00 – 0x7f	0x0
		6 5:0	correction polarity correction amplitude	0=Pos, 1=Neg 0=No correction LSB=0.5 mV	

Table 21: GBL CFG CTR 0 : Control Logic Settings

ID of register	GBL CFG CTR 0	Size	16 bits
Address	0x00000081	Read/Write	Read/Write
typedef	cfg ctr 0 t		

Bits	Name	Description	State/Range	Sleep
15:13	PS	Pulse Stretcher control. From 1 to 8 clock cycles	0-7 0=1 Clock cycle 7=8 Clock cycles	0
12:3		Unused		0
2	SyncLevel Enable	Switch the input synchronizer from edge to level mode	0=edge 1=level	0
1	ST	Self Trigger	0 = disable 1 = enable	0
0	DDR	Set the trigger output mode (DDR/SDR)	0 = srd 1 = ddr	0

Table 22: GBL CFG CTR 1: Data Packet Settings

ID of register	GBL CFG CTR 1	Size	16 bits
Address	0x00000082	Read/Write	Read/Write
typedef	cfg ctr 1 t		

Bits	Name	Description	State/Range	Sleep
15	P16	SPZS Mode : Partition summary only	0 = disable 1 = enable	0
14		Unused		0
13:10	PAR	SPZS Mode : max. no. of partitions 1-16	0-15	0
9		Unused		0
8	DT	Data Type : SPZS Mode enable	0 = disable 1 = enable	0
7	SZP	Suppress zero data packets	0 = disable 1 = enable	0
6	SZD	Suppress zero data fields.	0 = disable 1 = enable	0
5:4	TT	Time Tag format	00 = EC+BC 01 = EC 10 = BC 11 = (EC+BC)	00
3		Unused		0
2:1	ECb	Event Counter bytes	00 = 1B 01 = 2B 10 = 3B 11 = 1B	00
0	BCb	Bunch Counter bytes	0 = 2B 1 = 3B	0

Table 23: GBL CFG CTR 2 : Front End settings

ID of register	GBL CFG CTR 2	Size	16 bits
Address	0x00000083	Read/Write	Read/Write
typedef	cfg ctr 2 t		

Bits	Name	Description	State/Range	Sleep
15:8		Unused		0
7:5	TP FE	Front end peaking time	000 = 25 ns 001 = 50 ns 011 = 75 ns 111 = 100 ns	0
4:2	RES PRE	Preamplifier Resistance set	001 for High gain 010 for Middle gain 100 for Low gain	001
1:0	CAP PRE	Preamplifier Capacity set	00 for High gain 01 for Middle gain 11 for Low gain	00

Table 24: GBL CFG CTR 3 : CFD settings

ID of register	GBL CFG CTR 3	Size	16 bits
Address	0x00000084	Read/Write	Read/Write
typedef	cfg ctr 3 t		

Bits	Name	Description	State/Range	Sleep
15:10		Unused		0
9:6	PT	CFD Time Constant	0001 = 25 ns 0011 = 50 ns 0111 = 75 ns 1111 = 100 ns	0001
5	EN HYST	Arming comp. hysteresis	0 = disable 1 = enable	1
4	SEL POL	CFD input charge polarity	0 = positive (GEM) 1 = negative	0
3	Force En ZCC	Debug and calibration: force ZCC output (independent from arming comp.)	0 = disable 1 = enable	0
2	Force TH	Debug: force active ZCC threshold	0 = disable 1 = enable	0
1:0	SEL COMP MODE	CFD output mode	00 = normal 01 = arming 10 = ZCC 11 = 0	00

ID of register	GBL CFG CTR 4	Size	16 bits
Address	0x00000085	Read/Write	Read/Write
typedef	cfg ctr 4 t		

Bits	Name	Description	State/Range	Sleep
15:10		Unused		0
9:8	VREF ADC	ADC internal reference tuning (50 mV steps to adjust to 1.0 V during production calibration)	0-3	0x1
7	Mon Gain	Gain of ADC monitoring buffer	0 = Gain 1 1 = Gain 5	0
6		Unused		
5:0	Monitor Sel	Monitoring selection *Notes: Iref is always connected to Imon. Hence selections 1-16 are Iref + DAC indicated.* *Vmon = Calib Vstep dc level* *Vhigh when CalSelPol=0* *Vlow when CalSelPol=1* - - -	0 .. Imon = Iref 1 .. Imon = Calib IDC 2 .. Imon = Preamp InpTran 3 .. Imon = Preamp LC 4 .. Imon = Preamp SF 5 .. Imon = Shap FC 6 .. Imon = Shap Inpair 7 .. Imon = SD Inpair 8 .. Imon = SD FC 9 .. Imon = SD SF 10 .. Imon = CFD Bias1 11 .. Imon = CFD Bias2 12 .. Imon = CFD Hyst 13 .. Imon = CFD Ireflocal 14 .. Imon = CFD ThArm 15 .. Imon = CFD ThZcc 16 .. Imon = SLVS Ibias 32 .. Vmon = BGR 33 .. Vmon = Calib Vstep dc level (Vlow and Vhigh) 34 .. Vmon = Preamp Vref 35 .. Vmon = Vth Arm 36 .. Vmon = Vth ZCC 37 .. Vmon = V Tsens Int 38 .. Vmon = V Tsens Ext 39 .. Vmon = ADC_Vref 40 .. Vmon = ADC VinM 41 .. Vmon = SLVS Vref	0

Table 26: GBL CFG CTR 5 : Global reference current

ID of register	GBL CFG CTR 5	Size	16 bits
Address	0x00000086	Read/Write	Read/Write
typedef	cfg ctr 5 t		

Bits	Name	Description	State/Range	Sleep
15:6		Unused		0
5:0	Iref	Tuning of global reference current generated by Bandgap reference circuit. Target value: 10 uA. Nominal: 310nA/bit		0x20

Table 27: GBL CFG THR : Global Threshold settings

ID of register	GBL CFG THR	Size	16 bits
Address	0x00000087	Read/Write	Read/Write
typedef	cfg thr t		

Bits	Name	Description	State/Range	Sleep
15:8	ZCC DAC	ZCC global timing: nominal 0.5 mV/bit	0-0xff	0x0b
7:0	ARM DAC	Arming global threshold: nominal 2 mV/bit	0-0xff	0x20

Table 28: GBL CFG HYS : Global Threshold settings

ID of register	GBL CFG HYS	Size	16 bits
Address	0x00000088	Read/Write	Read/Write
typedef	cfg hyst t		

Bits	Name	Description	State/Range	Sleep
15:6		Unused		0
5:0	HYST DAC	Global hysteresis DAC: nominal 0.4mV/bit	0-0x3f	0x05

Table 29: GBL CFG LAT : Latency

ID of register	GBL CFG LAT	Size	16 bits
Address	0x00000089	Read/Write	Read/Write
typedef	cfg latency t		

Bits	Name	Description	State/Range	Sleep
9:0	LAT	Internal LV1A latency	0-1023	0

Table 30: GBL CFG CAL 0 : Calibration settings

ID of register	GBL CFG CAL 0	Size	16 bits
Address	0x0000008a	Read/Write	Read/Write
typedef	cfg cal 0 t		

Bits	Name	Description	State/Range	Sleep
15		Unused		0
14	CAL SEL POL	Calibration pulse polarity *Also selects dc pre-charge level when monitoring,* *Vhigh when CalSelPol=0* *Vlow when CalSelPol=1*	0 = positive 1 = negative	0
13:11	CAL PHI	Pulse phase in 1/320MHz (3.125 ns) delay	0-7 0 = No delay 7 = 21.87 ns	0
10	CAL EXT	External analog voltage step	0 = disable 1 = enable	0
9:2	CAL DAC	CAL DAC: amplitude of current pulse 256-CAL DAC: amplitude of voltage step	0-255	0
1:0	CAL MODE	Cal Pulse mode	00 : Disabled 01 : Voltage Pulse 1x : Current Pulse	0

Table 31: GBL CFG_CAL 1 : Calibration settings

ID of register	GBL CFG CAL 1	Size	16 bits
Address	0x0000008b	Read/Write	Read/Write
typedef	cfg cal 1 t		

Bits	Name	Description	State/Range	Sleep
15:11		Unused		0
10:9	CAL FS	Cal current pulse scale factor Q = CAL DUR[s] x CAL DAC x 10 nA x CAL FS [%]	00 : 25% 01 : 50% 10 : 75% 11 : 100%	
8:0	CAL DUR	Cal pulse duration in 40 MHz clock cycles	0-0x1ff	0x1ff

Table 32: GBL CFG BIAS 0 : Biasing settings

ID of register	GBL CFG BIAS 0	Size	16 bits
Address	0x0000008c	Read/Write	Read/Write
typedef	cfg bias 0 t		

Bits	Name	Description	State/Range	Sleep
15:12		Unused		0
11:6	CFD DAC 2	CFD Bias2 (current)	0-0x3f	0x28
5:0	CFD DAC 1	CFD Bias1 (current)	0-0x3f	0x28

Table 33: GBL CFG BIAS 1 : Biasing settings

ID of register	GBL CFG BIAS 1	Size	16 bits
Address	0x0000008d	Read/Write	Read/Write
typedef	cfg bias 1 t		

Bits	Name	Description	State/Range	Sleep
15:14		Unused		0
13:8	PRE I BSF	Preamplifier Bias Source Follower (current)	0-0x3f	1 (2 uA)
7:0	PRE I BIT	Preamplifier Bias Input Transistor (current)	0-0xff	1 (1 uA)

Table 34: GBL CFG BIAS 2 : Biasing settings

ID of register	GBL CFG BIAS 2	Size	16 bits
Address	0x0000008e	Read/Write	Read/Write
typedef	cfg bias 2 t		

Bits	Name	Description	State/Range	Sleep
15:14		Unused		0
13:8	PRE I BLCC	Preamplifier Bias Leakage Compensation (current)	0-0x3f	15 (15 nA)
7:0	PRE VREF	Preamplifier Vref	0-0xff	86 (430 mV)

Table 35: GBL CFG BIAS 3 : Biasing settings

ID of register	GBL CFG BIAS 3	Size	16 bits
Address	0x0000008f	Read/Write	Read/Write
typedef	cfg bias 3 t		

Bits	Name	Description	State/Range	Sleep
15:8	SH I BFCAS	Shaper Folded Cascode (current)	0-0xff	1 (100 nA)
7:0	SH I BDIFF	Shaper Input Pair (current)	0-0xff	1 (100 nA)

Table 36: GBL CFG BIAS 4 : Biasing settings

ID of register	GBL CFG BIAS 4	Size	16 bits
Address	0x00000090	Read/Write	Read/Write
typedef	cfg bias 4 t		

Bits	Name	Description	State/Range	Sleep
15:14		Unused		0
13:8	SH I BFAMP	Shaper Feed Amplifier (current)	0-0x3f	1 (1 nA)
7:0	SD I BDIFF	SD Input Pair (current)	0-0xff	1 (100 nA)

Table 37: GBL CFG BIAS 5 : Biasing settings

ID of register	GBL CFG BIAS 5	Size	16 bits
Address	0x00000091	Read/Write	Read/Write
typedef	cfg bias 5 t		

Bits	Name	Description	State/Range	Sleep
15:14		Unused		0
13:8	SD I BSF	SD Source Follower (current)	0-0x3f	1 (2 uA)
7:0	SD I BFCAS	SD Folded Cascode (current)	0-0xff	1 (100 nA)

Table 38: GBL CFG RUN : SLEEP/RUN

ID of register	GBL CFG RUN	Size	1 bits
Address	0x0000ffff	Read/Write	Read/Write
typedef			

Bits	Name	Description	State/Range	Sleep
0	RUN	SLEEP/RUN mode	0 = SLEEP 1 = RUN	0

Table 39: HW ID ID : Hardware ID

ID of register	HW ID ID	Size	32 bits
Address	0x00010000	Read/Write	Read only
typedef			

Bits	Name	Description	State/Range	Sleep
31:0	ID	Device Hardware ID reg.	Reports 0x56464154 (ASCII 'VFAT') on read	0x56464154

Table 40: HW ID VER : Hardware version

ID of register	HW ID VER	Size	32 bits
Address	0x00010001	Read/Write	Read only
typedef			

Bits	Name	Description	State/Range	Sleep
31:0	VER	Hardware version	Reports 0x00030000 (V3.0.0) on read	0x00030000

Table 41: HW RW REG : General purpose reg.

ID of register	HW RW REG	Size	32 bits
Address	0x00010002	Read/Write	Read/Write
typedef			

Bits	Name	Description	State/Range	Sleep
31:0	RW REG	General purpose read/write register		0

Table 42: HW CHIP ID : Chip ID

ID of register	HW CHIP ID	Size	32 bits
Address	0x00010003	Read/Write	Read only
typedef			

Bits	Name	Description	State/Range	Sleep
31:0	CHIP ID	CHIP ID from eFuses		0

Table 43: HW PROG : eFuse Program

ID of register	HW PROG	Size	32 bits
Address	0x00010004	Read/Write	Write only
typedef			

Bits	Name	Description	State/Range	Sleep
31:19		Unused		
18:8	PRG TIME	Program time in 25 ns units	0-0x7ff	
7:5		Unused		
4:0	PRG BIT ADD	Address of the bit to be programmed	0-0x1f	

Table 44: ADC READ 0 : Primary ADC read, ADC0 (using the internal reference).

ID of register	ADC READ 0	Size	10 bits
Address	0x00020000	Read/Write	Read only
typedef			

Bits	Name	Description	State/Range	Sleep
9:0	ADC 0	On read : triggers 3 conversions at 1 us intervals, returns result of the last conversion.		

Table 45: ADC READ 1 : ADC 1 (using the external reference)

ID of register	ADC READ 1	Size	10 bits
Address	0x00020001	Read/Write	Read only
typedef			

Bits	Name	Description	State/Range	Sleep
9:0	ADC 1	On read : triggers 3 conversions at 1 us intervals, returns result of the last conversion.		

8. POWER CONSUMPTION

The VFAT3 power supply voltage is 1.2 V for both analog and digital power domains. The power consumption is as shown in

Table 46: Power Consumption

	SLEEP Mode		RUN Mode	
	mA	mW	mA	mW
Analog	74	89	139	167
Digital	50	60	67	80
Total	124	149	206	247

9. PROCEDURES

9.1 Calibration Procedure

Test procedure for the Calibration-Bias-Monitoring of VFAT3 chip
Equipment: external high precision voltmeter.

9.1.1 Measuring the Bandgap voltage

The bandgap voltage (V_BGR, Figure 17) can be measured directly by an external multi-meter on pin V_BGR.
NOTE: the nominal value is 300mV.

9.1.2 Measuring Buffer Offsets in the Monitoring path

In the monitoring section (Figure 18) there are three buffers; two of them are used to drive the internal ADCs while a third one is used to provide the monitored quantity on an output pad (Vmon). It is important to verify the reliability of the buffer and this test can be done exploiting the measurement of the band gap reference. To accomplish this task:
1- Set the Monitor_Sel bits of the GBL_CFG_CTR_4 register equal to 32 (Vmon = VBGR)
2- By means of the V_BGR pad measure the band gap reference with the external voltmeter.

By comparing the two measurements, it is possible to measure the offset introduced by the buffer. Simulation shows it to be lower than 500uV. If the measured offset is higher than 2mV then it must not be neglected.

9.1.3 Iref

Iref is the reference current generated by DAC "Iref" immediately after the bandgap (Figure 17). This current is used for all the other bias DACs. In order to monitor bias currents generated in the chip an external high precision 20kOhms resistor (Rext) is used (Figure 18). The voltage across Rext is internally multiplexed and can be read using the internal ADCs or using an external ADC connected to VMON.
To measure and adjust the reference current:
1- set the Monitor_Sel bits of the GBL_CFG_CTR_4 register equal to 0.
2- Measure externally the voltage on the 20kOhm resistor to evaluate the current (5uA => 100mV across the resistor) .
3- If the measured current is different from the nominal 5uA change the Iref bits in the GBL_CFG_CTR_5 register until the set point value is reached.

NOTE: the default value of the Iref bits is 0x20, in the step 3 do not start from 0 but change the value around the default one.

9.1.4   *Calibrating the internal ADCs*

After the measurement of the main quantities used in the bias the internal ADCs can be calibrated.

A. Tuning of internal ADC0 voltage reference:

1- Set the Monitor_Sel bits of the GBL_CFG_CTR_4 (Table 25) register equal to 39 (ADC_Vref)
2- Change the VREF_ADC bits of the GBL_CFG_CTR_4 register from 0 to 3 (nominal step ~ 50 mV)
3- For each VREF_ADC word measure the reference voltage by means of Vmon test point.
4- Choose the VREF_ADC word to have the closest value to 1V (store this value in the database)

B. Internal ADC calibration:

1- Set Monitor_Sel bits of the GBL_CFG_CTR_4 register equal to 2 (IMON=Preamp_Inp_Tran)
2- Set 2 different values(i.e. "0" and "250") of the DAC Preamp_BiasInputTransistor (GBL_CFG_BIAS_1[7:0])
3- Measure the 2 voltages both with the internal ADC and with the external voltmeter by means of Vmon test point.

For each measurement we have a set of (W,V) where W is the conversion word provided by the internal ADC and V is the voltage measured by the external equipment:
- (W1,V1) set relative to measurement for the 1st value
- (W2,V2) set relative to measurement for the 2nd value

ADC gain: $G = (V2-V1)/(W2-W1)$
ADC offset: $Q = V1-G*W1$
Conversion law: $Vin = G*W+Q$

Repeat the calibration procedure for the internal ADC with the external reference (note that the final values for the conversion law must be different from the other ones because the external ADC reference is fixed and equal to AVDD = 1.2V).

The extracted values (G0, Q0, G1, Q1) must be stored in the database.

9.1.5   *DAC scans*

Once the internal ADCs have been calibrated the bias DACs can be characterized. Referring to the registers GBL_CFG_BIAS in section 7.4 ; for each configuration word the correspondent voltage/current can be read. In this phase it is important to consider the scale factors (shown in the monitoring tables Table 12, Table 13 and Table 14) .

NOTE: For the DACs that control the SLVS driver, do not start the from zero but change the values around the default one in order to tune the bias current and the reference voltage in case of differences between actual and nominal values.

9.2   Calibration of Zero Crossing Comparator (ZCC)

This procedure is based on the measurement of the channel delay, described in 9.2.1.
- **Phase 1: coarse tuning.** Assuming that for Q_{in} > 10 fC the pulse delay is closed to the asymptotic value, we search for the value of ZCC local DAC that minimizes the delay difference in case of a small charge respect to the large charge delay:
    1. Set a relatively high pulse charge Q_{big} (11 fC)
    2. Measure the delay between the CFD output and the calibration pulse. We define it as reference delay: T_{ref}
    3. Set a relatively low pulse charge Q_{small} (0.9 fC)
    4. Search ZCC local threshold (LDAC_coarse) that minimizes the time difference respect to T_{ref} (for instance using dichotomic search algorithm)
- **Phase 2: fine tuning.** Using LDAC_coarse as starting point, we search for the LDAC value that minimizes the delay difference respect to T_{ref} in a charge range around Q_{small}, in order to have the flattest delay distribution in the lower charge range:
    1. Scan Q_{in} in the range (0.5 fC ÷ 2.5 fC)
    2. Make the sum (S_{del}) of the differences to T_{ref} of the measured delay for each Q_{in}
    3. Search ZCC LDAC that minimizes S_{del}.

9.2.1   *Measurement of Channel Delay*

It is possible to indirectly measure the channel delay using the feature that allows to control the test pulse phase with steps of 25ns/8 = 3.125 ns.
1. Set the chip in "Self Trigger Mode" and "Pulse Stretcher" to "1 clock cycle" (Register GBL_CFG_CTR_0)
2. Send test pulses every 2^9 = 512 clock cycles: in this way the 9 LSB bits of the event time stamp are the same
3. Changing the phase of the test pulse it is possible to identify the crossing to the next BX
4. The total delay can be evaluated as in the example in Figure: the crossing to the next BX is when the pulse phase *nphase* goes from 4 to 5. The delay is then n*25ns + (8-nphase)*3.125 ns, where in this example n=4 and *nphase* =4
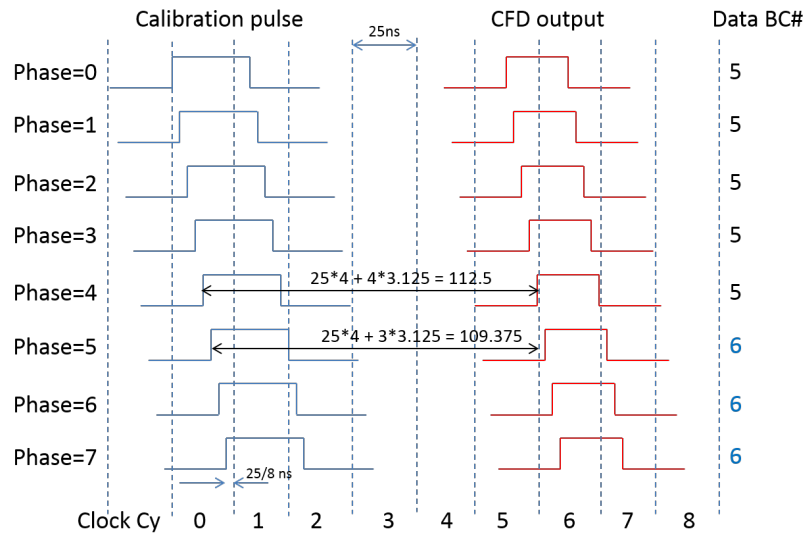
Figure 39: Example of time measurement

10. PRODUCTION TEST OPTIONS

Many of the VFAT3 operational functions and performance characteristics can be determined during the production test phase by normal operation of the chip routines, performing s-curves etc.

The basic operation of the digital section can be checked in this way. However production faults may still exist even with an operational chip due to the triple redundancy voting circuits that can hide non functional flip flops.

VFAT3 includes two features designed specifically to test the digital section during production and find otherwise hidden faults. These are :

- Scan path for combinatory and sequential logic cells.
- Built In Self Test (BIST) for memory testing

To guaranty the absence of faults in the digital section; the chip needs to run a specific tests based on test vectors generated by a dedicated Automatic Test Pattern Generator tool (ATPG) and the automatic test of the memories.

10.1 Scan Path

All Flip-Flops in the design have an input multiplexer and are connected together to build a shift register if the SCAN_EN signal is asserted (Scan Mode). When the chip is in Scan Mode the state of the Flip-Flops can be set shifting the required value into the scan chain by the SCAN_IN pin and the current state can be read back by the SCAN_OUT pin. Standard test procedure requires:
1- Assert SCAN_EN, shift in the test vector, set primary inputs
2- De-assert SCAN_EN, apply the required number of clock pulses
3- Assert SCAN_EN, shift out chain state, read primary outputs and compare results with test vector
To speed up the test usually the step 3 and 1 are done at the same time, shifting in a new test vector while shifting out the result of the previous one.
In VFAT3 design Flip-Flops are split in six chains, partitioning them based on clock domains and triplication.
All Flip-Flops of one chain have a common SCAN_EN signal and a common clock tree, not shared with Flip-Flops on other chains.

10.2 BIST (Built In Self Test)

The BIST has been implemented replacing each standard memory block with an instrumented block, made by the standard block surrounded by the BIST logic. The BIST logic implements the "Extended March C-" algorithm that can be synthetically described as:
$\{\updownarrow (w0); \Uparrow (r0, w1, r1); \Uparrow (r1, w0); \Downarrow (r0, w1); \Downarrow (r1, w0); \updownarrow (r0)\}$
That means for the first three terms:
- Write "0" in all locations regardless of the address increment/decrements
- for each memory location read "0", write "1" and read "1" increasing the address

- for each memory location read "1" and write "0" increasing the address

This algorithm is able to detect most of the potential faults in the SRAM block.

The testing logic is designed to allow daisy chain of memory blocks to minimize the number of external dedicated pads and adds four pins to the SDRAM block:

- **BIST_RUN_IN**: when read at "1" for three consecutive clock cycles the BIST logic starts to run the test until the end or BIST_start is released to "0"

- **BIST_RUN_OUT**: set to "1" when test is finished and released to "0" when BIST_RUN_IN is released

- **BIST_ERR_IN**: Connected to the previously memory block in the chain

- **BIST_ERR_OUT**: Set to "1" while test is running. After test end it is set to "1" if an error is detected by the current block or one of the previous blocks in the chain.

At top level pad BIST_START is connected to BIST_RUN_IN of the first block of the chain, pads BIST_END and BIST_OK are connected to BIST_RUN_OUT and BIST_ERR_OUT of the last block of the chain.

NOTE: due to a bug in the RTL code, faults in the memory blocks are not propagated to the output pad BIST_OK. The only mode to know if a BIST block detected a fault is to count the number of clock cycles from start to end of the test (from BIST_START to BIST_END). If a fault is detected in any memory block, the check on it is aborted, resulting in a shorter running time.

11.   VFAT3 DIE SIZES

VFAT3 was designed in 2, almost identical versions; VFAT3 and VFAT3prot. The "prot" version has increased input protection for use with gaseous detectors. The VFAT3 version is more suitable to silicon detectors. The die sizes for both are shown in Figure 32 .
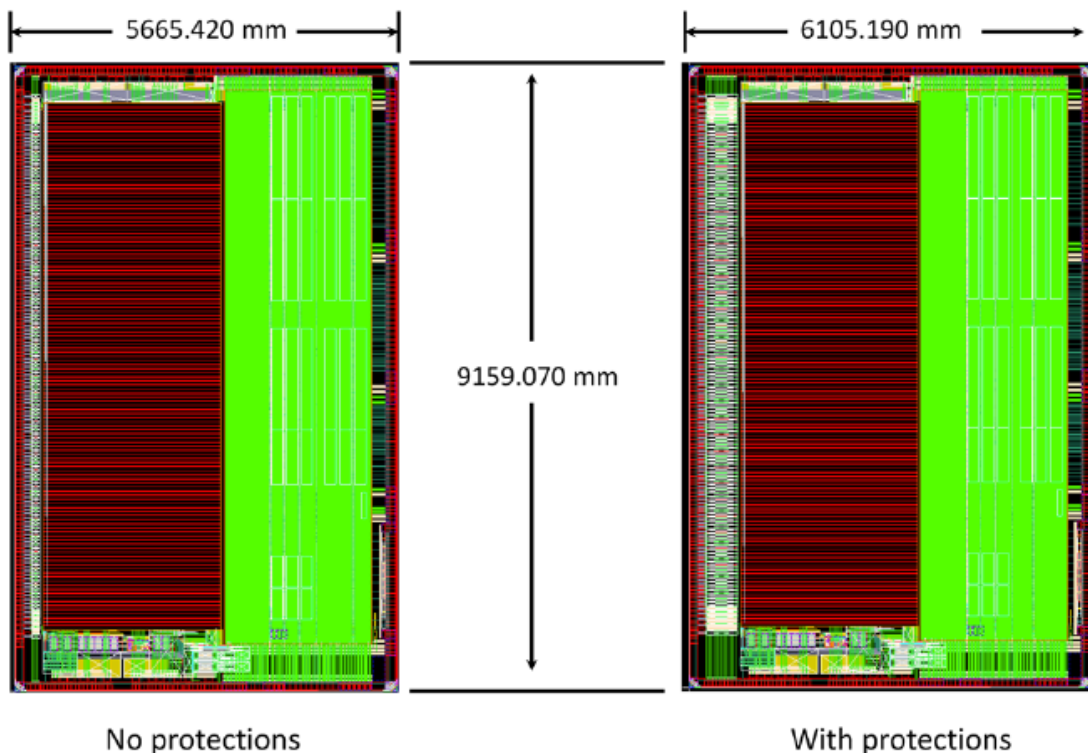
Figure 40: Die sizes for VFAT3 and VFAT3prot

12.   PADS

There are 520 pads on VFAT3. However many of these pads are used for testability purposes and are not need for the final application. The different type of functions the pads take on are

Tables of the VFAT3 pads, their function and location coordinates are in Table 47 to Table 51 . The function of the pad is listed as "Operational" (required for operation of VFAT3), "Production"(required for production testing) and Debug/Characterisation (only needed during the testability phase and not for final operation).

Table 47: VFAT3 pads; North side (West to East)

pin #		Operational	Production	Debug, Characterication	Description	PCB net	Connector	X [µm]	Y [µm]
	North side (West to East)								
0	VDD_PROT	x	x	x	VDD for protection diodes	AVDD 1.2V	GEB	200	9068.2
1	GND_PROT	x	x	x	GND for protection diodes	AGND	GEB	260	9068.2
2	GND_PROT	x	x	x	GND for protection diodes	AGND	GEB	320	9068.2
3	tbuff_ibias			x	FE test channel bias(load res to GND)	tbuff_ibias	on board	435	9068.2
4	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	495	9068.2
5	GND_FE	x	x	x	Front end return	AGND	GEB	555	9068.2
6	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	615	9068.2
7	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	675	9068.2
8	GND_FE	x	x	x	Front end return	AGND	GEB	735	9068.2
9	PreAmpOut			x	Test channel preamp out	PreAmpOut	testpoint	795	9068.2
10	Shaperin			x	Test channel Shaper in	Shaperin	lemo	855	9068.2
11	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	915	9068.2
12	GND_FE	x	x	x	Front end return	AGND	GEB	975	9068.2
13	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	1035	9068.2
14	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	1095	9068.2
15	GND_FE	x	x	x	Front end return	AGND	GEB	1155	9068.2
16	ShaperOut			x	Test channel shaper out	ShaperOut	testpoint	1215	9068.2
17	DiffBuffIn			x	Test channel DiffBuff in	DiffBuffIn	lemo	1275	9068.2
18	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	1335	9068.2
19	GND_FE	x	x	x	Front end return	AGND	GEB	1395	9068.2
20	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	1455	9068.2
21	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	1515	9068.2
22	GND_FE	x	x	x	Front end return	AGND	GEB	1575	9068.2
23	DiffBuffOutp			x	Test channel DiffBuff outp	DiffBuffOutp	testpoint	1635	9068.2
24	DiffBuffOutn			x	Test channel DiffBuff outn	DiffBuffOutn	testpoint	1695	9068.2
25	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	1755	9068.2
26	CFDInn			x	Test channel CFD inn	CFDInn	lemo	1830	9068.2
27	CFDInp			x	Test channel CFD inp	CFDInp	lemo	1890	9068.2
28	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	1950	9068.2
29	GND_CFD	x	x	x	CFD return	AGND	GEB	2010	9068.2
30	AVDD_CFD	x	x	x	CFD analog VDD	AVDD	GEB	2070	9068.2
31	GND_CFD	x	x	x	CFD return	AGND	GEB	2130	9068.2
32	AVDD_CFD	x	x	x	CFD analog VDD	AVDD	GEB	2190	9068.2
33	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	2250	9068.2
34	GND_CFD	x	x	x	CFD return	AGND	GEB	2310	9068.2
35	AVDD_CFD	x	x	x	CFD analog VDD	AVDD	GEB	2370	9068.2
36	GND_CFD	x	x	x	CFD return	AGND	GEB	2430	9068.2
37	AVDD_CFD	x	x	x	CFD analog VDD	AVDD	GEB	2490	9068.2
38	DVSS_CFD	x	x	x	CFD digital return	AGND	GEB	2685	9068.2
39	DVDD_CFD	x	x	x	CFD digital VDD	AVDD	GEB	2745	9068.2
40	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	2805	9068.2
41	DVSS_CFD	x	x	x	CFD digital return	AGND	GEB	2865	9068.2
42	DVDD_CFD	x	x	x	CFD digital VDD	AVDD	GEB	2925	9068.2
43	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	3005	9068.2
44	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	3087.175	9068.2
45	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	3165	9068.2
46	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	3245	9068.2
47	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	3325	9068.2
48	VDD_IO	x	x	x	IO ring VDD	VDD_IO	GEB	3405	9068.2
49	CFDOut_pad			x	Test channel CFD out	CFDOut_pad	testpoint	3485	9068.2
50	SCAN_IN0_A_pad		x	x	Scan chain input	SCAN_IN0_A_pad	GEB	3565	9068.2
51	SCAN_IN0_B_pad		x	x	Scan chain input	SCAN_IN0_B_pad	GEB	3645	9068.2
52	SCAN_IN0_C_pad		x	x	Scan chain input	SCAN_IN0_C_pad	GEB	3725	9068.2
53	SCAN_EN0_A_pad		x	x	Scan chain enable	SCAN_EN0_A_pad	GEB	3805	9068.2
54	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	3885	9068.2
55	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	3965	9068.2
56	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	4045	9068.2
57	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	4125	9068.2
58	SCAN_EN0_B_pad		x	x	Scan chain enable	SCAN_EN0_B_pad	GEB	4205	9068.2
59	SCAN_EN0_C_pad		x	x	Scan chain enable	SCAN_EN0_C_pad	GEB	4285	9068.2
60	SCAN_OUT0_A_pad		x	x	Scan chain out	SCAN_OUT0_A_pad	GEB	4365	9068.2
61	SCAN_OUT0_B_pad		x	x	Scan chain out	SCAN_OUT0_B_pad	GEB	4445	9068.2
62	SCAN_OUT0_C_pad		x	x	Scan chain out	SCAN_OUT0_C_pad	GEB	4525	9068.2
63	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	4605	9068.2
64	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	4687.175	9068.2
65	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	4765	9068.2
66	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	4845	9068.2
67	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	4925	9068.2
68	VDD_IO	x	x	x	IO ring VDD	VDD_IO	GEB	5005	9068.2

Table 48: VFAT3 pads; East side (North to South)

#	Name				Description	Signal	Type		Coord
	East side (North to south)								
69	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	8790
70	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	8710
71	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	5573.2	8632.175
72	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	5573.2	8550
73	VDD_IO	x	x	x	IO ring VDD	VDD_IO	GEB	5573.2	8470
74	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	8390
75	SCAN_IN1_A_pad		x	x	Scan chain input	SCAN_IN1_A_pad	GEB	5573.2	8310
76	SCAN_IN1_B_pad		x	x	Scan chain input	SCAN_IN1_B_pad	GEB	5573.2	8230
77	SCAN_IN1_C_pad		x	x	Scan chain input	SCAN_IN1_C_pad	GEB	5573.2	8150
78	SCAN_EN1_A_pad		x	x	Scan chain enable	SCAN_EN1_A_pad	GEB	5573.2	8070
79	SCAN_EN1_B_pad		x	x	Scan chain enable	SCAN_EN1_B_pad	GEB	5573.2	7990
80	SCAN_EN1_C_pad		x	x	Scan chain enable	SCAN_EN1_C_pad	GEB	5573.2	7910
81	SCAN_OUT1_A_pad		x	x	Scan chain output	SCAN_OUT1_A_pad	GEB	5573.2	7830
82	SCAN_OUT1_B_pad		x	x	Scan chain output	SCAN_OUT1_B_pad	GEB	5573.2	7750
83	SCAN_OUT1_C_pad		x	x	Scan chain output	SCAN_OUT1_C_pad	GEB	5573.2	7670
84	HDLC_ADDRESS_pad<0>		x	x	HDLC address (internal pull down resistor)	HDLC_ADDRESS_pad<0>	test	5573.2	7580
85	HDLC_ADDRESS_pad<1>		x	x	HDLC address (internal pull down resistor)	HDLC_ADDRESS_pad<1>	test	5573.2	7500
86	HDLC_ADDRESS_pad<2>		x	x	HDLC address (internal pull down resistor)	HDLC_ADDRESS_pad<2>	test	5573.2	7420
87	HDLC_ADDRESS_pad<3>		x	x	HDLC address (internal pull down resistor)	HDLC_ADDRESS_pad<3>	test	5573.2	7340
88	HDLC_ADDRESS_pad<4>		x	x	HDLC address (internal pull down resistor)	HDLC_ADDRESS_pad<4>	test	5573.2	7260
89	HDLC_ADDRESS_pad<5>		x	x	HDLC address (internal pull down resistor)	HDLC_ADDRESS_pad<5>	test	5573.2	7180
90	HDLC_ADDRESS_pad<6>		x	x	HDLC address (internal pull down resistor)	HDLC_ADDRESS_pad<6>	test	5573.2	7100
91	HDLC_ADDRESS_pad<7>		x	x	HDLC address (internal pull down resistor)	HDLC_ADDRESS_pad<7>	test	5573.2	7020
92	BIST_OK_pad		x	x	BIST ok	BIST_OK_pad	GEB	5573.2	6940
93	BIST_END_pad		x	x	BIST end	BIST_END_pad	GEB	5573.2	6860
94	BIST_START_pad		x	x	BIST start	BIST_START_pad	GEB	5573.2	6780
95	VDD_IO	x	x	x	IO ring VDD	VDD_IO	GEB	5573.2	6700
96	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	6620
97	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	6540
98	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	6460
99	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	5573.2	6382.175
100	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	5573.2	6300
101	TP_IN_SE_pad			x	Digital test and debug signals	TP_IN_SE_pad	test	5573.2	6220
102	TP_IN_SI_pad			x	Digital test and debug signals	TP_IN_SI_pad	test	5573.2	6140
103	TP_ADC_RESULT_pad<0>			x	Digital test and debug signals	TP_ADC_RESULT_pad<0>	test	5573.2	6060
104	TP_ADC_RESULT_pad<1>			x	Digital test and debug signals	TP_ADC_RESULT_pad<1>	test	5573.2	5980
105	TP_ADC_RESULT_pad<2>			x	Digital test and debug signals	TP_ADC_RESULT_pad<2>	test	5573.2	5900
106	TP_ADC_RESULT_pad<3>			x	Digital test and debug signals	TP_ADC_RESULT_pad<3>	test	5573.2	5820
107	TP_ADC_RESULT_pad<4>			x	Digital test and debug signals	TP_ADC_RESULT_pad<4>	test	5573.2	5740
108	TP_ADC_RESULT_pad<5>			x	Digital test and debug signals	TP_ADC_RESULT_pad<5>	test	5573.2	5660
109	TP_ADC_RESULT_pad<6>			x	Digital test and debug signals	TP_ADC_RESULT_pad<6>	test	5573.2	5580
110	TP_ADC_RESULT_pad<7>			x	Digital test and debug signals	TP_ADC_RESULT_pad<7>	test	5573.2	5500
111	TP_ADC_RESULT_pad<8>			x	Digital test and debug signals	TP_ADC_RESULT_pad<8>	test	5573.2	5420
112	TP_ADC_RESULT_pad<9>			x	Digital test and debug signals	TP_ADC_RESULT_pad<9>	test	5573.2	5340
113	TP_ADC_SELECT_pad			x	Digital test and debug signals	TP_ADC_SELECT_pad	test	5573.2	5260
114	TP_ADC_SOC_pad			x	Digital test and debug signals	TP_ADC_SOC_pad	test	5573.2	5180
115	TP_ADC_CTRL_pad<0>			x	Digital test and debug signals	TP_ADC_CTRL_pad<0>	test	5573.2	5100
116	TP_ADC_CTRL_pad<1>			x	Digital test and debug signals	TP_ADC_CTRL_pad<1>	test	5573.2	5020
117	TP_DF_DTS_pad			x	Digital test and debug signals	TP_DF_DTS_pad	test	5573.2	4940
118	TP_DF_TXD_pad<7>			x	Digital test and debug signals	TP_DF_TXD_pad<7>	test	5573.2	4860
119	TP_DF_TXD_pad<6>			x	Digital test and debug signals	TP_DF_TXD_pad<6>	test	5573.2	4780
120	TP_DF_TXD_pad<5>			x	Digital test and debug signals	TP_DF_TXD_pad<5>	test	5573.2	4700
121	VSS	x	x		Digital VSS for IO-Ring	DGND	GEB	5573.2	4620
122	VDD_IO	x	x		IO ring VDD	VDD_IO	GEB	5573.2	4540
123	VDD	x	x		Digital VDD for the IO-Ring	DVDD	GEB	5573.2	4460
124	VDD	x	x		Digital VDD for the IO-Ring	DVDD	GEB	5573.2	4377.825
125	VSS	x	x		Digital VSS for IO-Ring	DGND	GEB	5573.2	4300
126	VSS	x	x		Digital VSS for IO-Ring	DGND	GEB	5573.2	4220
127	TP_DF_TXD_pad<4>			x	Digital test and debug signals	TP_DF_TXD_pad<4>	test	5573.2	4150
128	TP_DF_TXD_pad<3>			x	Digital test and debug signals	TP_DF_TXD_pad<3>	test	5573.2	4090
129	TP_DF_TXD_pad<2>			x	Digital test and debug signals	TP_DF_TXD_pad<2>	test	5573.2	4030
130	TP_DF_TXD_pad<1>			x	Digital test and debug signals	TP_DF_TXD_pad<1>	test	5573.2	3970
131	TP_DF_TXD_pad<0>			x	Digital test and debug signals	TP_DF_TXD_pad<0>	test	5573.2	3910
132	TP_DF_CTRL_pad<0>			x	Digital test and debug signals	TP_DF_CTRL_pad<0>	test	5573.2	3850
133	TP_DF_CTRL_pad<1>			x	Digital test and debug signals	TP_DF_CTRL_pad<1>	test	5573.2	3790
134	TP_CI_CAL_pad			x	Digital test and debug signals	TP_CI_CAL_pad	test	5573.2	3730
135	TP_CI_LV1A_pad			x	Digital test and debug signals	TP_CI_LV1A_pad	test	5573.2	3670
136	TP_CI_RESYNC_pad			x	Digital test and debug signals	TP_CI_RESYNC_pad	test	5573.2	3610
137	TP_CI_BC0_pad			x	Digital test and debug signals	TP_CI_BC0_pad	test	5573.2	3550
138	TP_CI_EC0_pad			x	Digital test and debug signals	TP_CI_EC0_pad	test	5573.2	3490
139	TP_CI_CTRL_pad<0>			x	Digital test and debug signals	TP_CI_CTRL_pad<0>	test	5573.2	3430
140	TP_CI_CTRL_pad<1>			x	Digital test and debug signals	TP_CI_CTRL_pad<1>	test	5573.2	3370
141	SPI_DO_pad			x	Digital test and debug signals	SPI_DO_pad	test	5573.2	3310
142	SPI_DI_pad			x	Digital test and debug signals	SPI_DI_pad	test	5573.2	3250
143	SPI_EN_pad			x	Digital test and debug signals	SPI_EN_pad	test	5573.2	3190
144	SPI_CLK_pad			x	Digital test and debug signals	SPI_CLK_pad	test	5573.2	3130
145	SCAN_CLK0_EN_pad		x		Scan chain clock enable	SCAN_CLK0_EN_pad	GEB	5573.2	3070
146	SCAN_CLK_pad		x		Scan chain clock	SCAN_CLK_pad	GEB	5573.2	3010
147	VSS	x	x		Digital VSS for IO-Ring	DGND	GEB	5573.2	2940
148	VDD_EFUSE	x	x	x	VDD for Efuse	VDD_EFUSE	GEB	5573.2	2870
149	VDD_IO	x	x	x	IO ring VDD	VDD_IO	GEB	5573.2	2790
150	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	2730
151	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	2670
152	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	2610
153	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	5573.2	2550
154	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	5573.2	2490
155	VDD_SLVS	x	x	x	SLVS VDD	DVDD	GEB	5573.2	2405
156	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	2345
157	TU_SoT_p	x	x	x	Trigger start of transmission	T_SoT	GEB	5573.2	2285
158	TU_SoT_n	x	x	x	Trigger start of transmission	T_SoTb	GEB	5573.2	2225
159	TU_TXD_p<0>	x	x	x	Trigger bits	T<0>	GEB	5573.2	2165
160	TU_TXD_n<0>	x	x	x	Trigger bits	Tb<0>	GEB	5573.2	2105
161	TU_TXD_p<1>	x	x	x	Trigger bits	T<1>	GEB	5573.2	2045
162	TU_TXD_n<1>	x	x	x	Trigger bits	Tb<1>	GEB	5573.2	1985
163	TU_TXD_p<2>	x	x	x	Trigger bits	T<2>	GEB	5573.2	1925
164	TU_TXD_n<2>	x	x	x	Trigger bits	Tb<2>	GEB	5573.2	1865
165	TU_TXD_p<3>	x	x	x	Trigger bits	T<3>	GEB	5573.2	1805
166	TU_TXD_n<3>	x	x	x	Trigger bits	Tb<3>	GEB	5573.2	1745
167	TU_TXD_p<4>	x	x	x	Trigger bits	T<4>	GEB	5573.2	1685
168	TU_TXD_n<4>	x	x	x	Trigger bits	Tb<4>	GEB	5573.2	1625
169	TU_TXD_p<5>	x	x	x	Trigger bits	T<5>	GEB	5573.2	1565
170	TU_TXD_n<5>	x	x	x	Trigger bits	Tb<5>	GEB	5573.2	1505
171	TU_TXD_p<6>	x	x	x	Trigger bits	T<6>	GEB	5573.2	1445
172	TU_TXD_n<6>	x	x	x	Trigger bits	Tb<6>	GEB	5573.2	1385
173	TU_TXD_p<7>	x	x	x	Trigger bits	T<7>	GEB	5573.2	1325
174	TU_TXD_n<7>	x	x	x	Trigger bits	Tb<7>	GEB	5573.2	1265
175	TXD_p	x	x	x	E-links	TXD	GEB	5573.2	1205
176	TXD_n	x	x	x	E-links	TXDb	GEB	5573.2	1145
177	RXD_p	x	x	x	E-links	RXD	GEB	5573.2	1085
178	RXD_n	x	x	x	E-links	RXDb	GEB	5573.2	1025
179	RXCLK_p	x	x	x	E-links	RXCLK	GEB	5573.2	965
180	RXCLK_n	x	x	x	E-links	RXCLKb	GEB	5573.2	905
181	VDD_SLVS	x	x	x	SLVS VDD	DVDD	GEB	5573.2	845
182	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	785
183	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	5573.2	710
184	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	5573.2	650
185	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	590
186	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5573.2	530

Table 49: VFAT3 pads; South side (East to West)

	South side (East to West)								
187	VDD_IO	x	x	x	IO ring VDD	VDD_IO	GEB	5225	41.8
188	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5145	41.8
189	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	5065	41.8
190	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	4985	41.8
191	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	4907.175	41.8
192	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	4825	41.8
193	TP_SC_RES_pad			x	Digital test and debug signals	TP_SC_RES_pad	test	4745	41.8
194	TP_SC_RXD_pad			x	Digital test and debug signals	TP_SC_RXD_pad	test	4665	41.8
195	TP_SC_RX_DTS_pad			x	Digital test and debug signals	TP_SC_RX_DTS_pad	test	4585	41.8
196	TP_SC_TX_ACK_pad			x	Digital test and debug signals	TP_SC_TX_ACK_pad	test	4505	41.8
197	TP_SC_TXD_pad			x	Digital test and debug signals	TP_SC_TXD_pad	test	4425	41.8
198	TP_SC_TX_DTS_pad			x	Digital test and debug signals	TP_SC_TX_DTS_pad	test	4345	41.8
199	TP_SC_CTRL_pad<1>			x	Digital test and debug signals	TP_SC_CTRL_pad<1>	test	4265	41.8
200	TP_SC_CTRL_pad<0>			x	Digital test and debug signals	TP_SC_CTRL_pad<0>	test	4185	41.8
201	TP_MON_CLK_EN_pad			x	Digital test and debug signals	TP_MON_CLK_EN_pad	test	4105	41.8
202	TP_MON_CLK_pad			x	Digital test and debug signals	TP_MON_CLK_pad	test	4025	41.8
203	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	3945	41.8
204	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	3865	41.8
205	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	3785	41.8
206	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	3705	41.8
207	BOR_DISABLE_pad		x	x	Power on reset signal	BOR_DISABLE_pad	test	3635	41.8
208	RST_TEST_MODE_pad		x	x	Power on reset signal	RST_TEST_MODE_pad	GEB	3575	41.8
209	EXT_RESET_pad	x	x	x	Hard reset	ReH	GEB	3515	41.8
210	POR_DISABLE_pad		x	x	Power on reset signal	POR_DISABLE_pad	test	3455	41.8
211	VDD_IO	x	x	x	IO ring VDD	VDD_IO	GEB	3395	41.8
212	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	3335	41.8
213	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	3275	41.8
214	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	3215	41.8
215	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	3155	41.8
216	VDD	x	x	x	Digital VDD for the IO-Ring	DVDD	GEB	3095	41.8
217	Ext_Vref_ADC1	x	x	x	ADC reference	Ext_Vref_ADC1	on board	3020	41.8
218	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	2960	41.8
219	DVDD_CFD	x	x	x	CFD digital VDD	AVDD	GEB	2900	41.8
220	DVSS_CFD	x	x	x	CFD digital return	AGND	GEB	2840	41.8
221	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	2780	41.8
222	Int_Vref_ADC0	x	x	x	ADC reference	Int_Vref_ADC0	testpoint	2720	41.8
223	Vmon		x	x	DAC voltages	Vmon	on board	2660	41.8
224	DVDD_CFD	x	x	x	CFD digital VDD	AVDD	GEB	2570	41.8
225	DVSS_CFD	x	x	x	CFD digital return	AGND	GEB	2510	41.8
226	VDD_TSENS_INT	x	x	x	VDD temp sensor	AVDD	GEB	2435	41.8
227	GND_CFD	x	x	x	CFD return	AGND	GEB	2375	41.8
228	V_Tsens_ext	x	x	x	Input for external temperature sensor	V_Tsens_ext	on board	2290	41.8
229	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	2230	41.8
230	GND_CFD	x	x	x	CFD return	AGND	GEB	2170	41.8
231	AVDD_CFD	x	x	x	CFD analog VDD	AVDD	GEB	2110	41.8
232	AVDD_CFD	x	x	x	CFD analog VDD	AVDD	GEB	2050	41.8
233	GND_CFD	x	x	x	CFD return	AGND	GEB	1990	41.8
234	VSS	x	x		Digital VSS for IO-Ring	DGND	GEB	1930	41.8
235	V_BGR			x	Bandgap reference voltage	V_BGR	testpoint	1870	41.8
236	AVDD_CFD	x	x	x	CFD analog VDD	AVDD	GEB	1810	41.8
237	GND_CFD	x	x	x	CFD return	AGND	GEB	1750	41.8
238	Ext_Iref			x	Reference current in case of non functional bandgap	Ext_Iref	on board	1530	41.8
239	En_ext_Iref			x	Reference current in case of non functional bandgap enable	En_ext_Iref	on board	1470	41.8
240	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	1410	41.8
241	GND_FE	x	x	x	Front end return	AGND	GEB	1350	41.8
242	Imon	x	x	x	DAC currents	Imon	on board	1275	41.8
243	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	1215	41.8
244	GND_FE	x	x	x	Front end return	AGND	GEB	1155	41.8
245	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	1095	41.8
246	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	1035	41.8
247	GND_FE	x	x	x	Front end return	AGND	GEB	975	41.8
248	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	915	41.8
249	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	855	41.8
250	GND_FE	x	x	x	Front end return	AGND	GEB	795	41.8
251	GND_FE	x	x	x	Front end return	AGND	GEB	735	41.8
252	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	675	41.8
253	VDD_FE	x	x	x	Front end VDD	AVDD	GEB	615	41.8
254	GND_FE	x	x	x	Front end return	AGND	GEB	555	41.8
255	VSS	x	x	x	Digital VSS for IO-Ring	DGND	GEB	495	41.8
256	extAC_pulse			x	External charge pulse input	extAC_pulse	lemo	435	41.8
257	GND_PROT	x	x	x	GND for protection diodes	AGND	GEB	320	41.8
258	GND_PROT	x	x	x	GND for protection diodes	AGND	GEB	260	41.8
259	VDD_PROT	x	x	x	VDD for protection diodes	AVDD 1.2V	GEB	200	41.8

Table 50: VFAT3 pads; West side gnd pads

		GROUND PINS								
260	VSS		x	x	x	Bias for IO-Ring	DGND	GEB	41.8	665
261	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	785
262	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	905
263	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	995
264	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1075
265	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1145
266	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1210
267	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1270
268	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1330
269	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1390
270	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1450
271	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1510
272	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1570
273	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1630
274	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1690
275	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1750
276	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1810
277	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1870
278	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1930
279	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	1990
280	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2050
281	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2110
282	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2170
283	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2230
284	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2290
285	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2350
286	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2410
287	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2470
288	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2530
289	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2590
290	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2650
291	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2710
292	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2770
293	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2830
294	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2890
295	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	2950
296	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3010
297	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3070
298	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3130
299	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3190
300	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3250
301	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3310
302	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3370
303	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3430
304	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3490
305	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3550
306	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3610
307	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3670
308	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3730
309	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3790
310	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3850
311	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3910
312	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	3970
313	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4030
314	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4090
315	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4150
316	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4210
317	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4270
318	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4330
319	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4390
320	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4450
321	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4510
322	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4570
323	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4630
324	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4690
325	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4750
326	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4810
327	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4870
328	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4930
329	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	4990
330	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5050
331	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5110
332	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5170
333	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5230
334	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5290
335	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5350
336	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5410
337	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5470
338	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5530
339	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5590
340	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5650
341	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5710
342	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5770
343	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5830
344	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5890
345	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	5950
346	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6010
347	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6070
348	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6130
349	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6190
350	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6250
351	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6310
352	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6370
353	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6430
354	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6490
355	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6550
356	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6610
357	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6670
358	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6730
359	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6790
360	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6850
361	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6910
362	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	6970
363	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7030
364	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7090
365	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7150
366	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7210
367	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7270
368	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7330
369	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7390
370	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7450
371	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7510
372	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7570
373	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7630
374	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7690
375	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7750
376	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7810
377	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7870
378	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7930
379	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	7990
380	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	8050
381	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	8110
382	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	8170
383	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	8230
384	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	8290
385	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	8355
386	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	8425
387	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	8505
388	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	8595
389	GND_FE		x	x	x	Channel input transistor return	AGND	GEB	41.8	8715
390	VSS		x	x	x	Bias for IO-Ring	DGND	GEB	41.8	8835

Table 51: VFAT3 pads; West side (South to North)

	West Side (South to North) Input channels								
391	IN0	x	x	x	Channel Input	IN0	GEM	169.8	815
392	IN1	x	x	x	Channel Input	IN1	GEM	169.8	935
393	IN2	x	x	x	Channel Input	IN2	GEM	169.8	1025
394	IN3	x	x	x	Channel Input	IN3	GEM	169.8	1105
395	IN4	x	x	x	Channel Input	IN4	GEM	169.8	1175
396	IN5	x	x	x	Channel Input	IN5	GEM	169.8	1240
397	IN6	x	x	x	Channel Input	IN6	GEM	169.8	1300
398	IN7	x	x	x	Channel Input	IN7	GEM	169.8	1360
399	IN8	x	x	x	Channel Input	IN8	GEM	169.8	1420
400	IN9	x	x	x	Channel Input	IN9	GEM	169.8	1480
401	IN10	x	x	x	Channel Input	IN10	GEM	169.8	1540
402	IN11	x	x	x	Channel Input	IN11	GEM	169.8	1600
403	IN12	x	x	x	Channel Input	IN12	GEM	169.8	1660
404	IN13	x	x	x	Channel Input	IN13	GEM	169.8	1720
405	IN14	x	x	x	Channel Input	IN14	GEM	169.8	1780
406	IN15	x	x	x	Channel Input	IN15	GEM	169.8	1840
407	IN16	x	x	x	Channel Input	IN16	GEM	169.8	1900
408	IN17	x	x	x	Channel Input	IN17	GEM	169.8	1960
409	IN18	x	x	x	Channel Input	IN18	GEM	169.8	2020
410	IN19	x	x	x	Channel Input	IN19	GEM	169.8	2080
411	IN20	x	x	x	Channel Input	IN20	GEM	169.8	2140
412	IN21	x	x	x	Channel Input	IN21	GEM	169.8	2200
413	IN22	x	x	x	Channel Input	IN22	GEM	169.8	2260
414	IN23	x	x	x	Channel Input	IN23	GEM	169.8	2320
415	IN24	x	x	x	Channel Input	IN24	GEM	169.8	2380
416	IN25	x	x	x	Channel Input	IN25	GEM	169.8	2440
417	IN26	x	x	x	Channel Input	IN26	GEM	169.8	2500
418	IN27	x	x	x	Channel Input	IN27	GEM	169.8	2560
419	IN28	x	x	x	Channel Input	IN28	GEM	169.8	2620
420	IN29	x	x	x	Channel Input	IN29	GEM	169.8	2680
421	IN30	x	x	x	Channel Input	IN30	GEM	169.8	2740
422	IN31	x	x	x	Channel Input	IN31	GEM	169.8	2800
423	IN32	x	x	x	Channel Input	IN32	GEM	169.8	2860
424	IN33	x	x	x	Channel Input	IN33	GEM	169.8	2920
425	IN34	x	x	x	Channel Input	IN34	GEM	169.8	2980
426	IN35	x	x	x	Channel Input	IN35	GEM	169.8	3040
427	IN36	x	x	x	Channel Input	IN36	GEM	169.8	3100
428	IN37	x	x	x	Channel Input	IN37	GEM	169.8	3160
429	IN38	x	x	x	Channel Input	IN38	GEM	169.8	3220
430	IN39	x	x	x	Channel Input	IN39	GEM	169.8	3280
431	IN40	x	x	x	Channel Input	IN40	GEM	169.8	3340
432	IN41	x	x	x	Channel Input	IN41	GEM	169.8	3400
433	IN42	x	x	x	Channel Input	IN42	GEM	169.8	3460
434	IN43	x	x	x	Channel Input	IN43	GEM	169.8	3520
435	IN44	x	x	x	Channel Input	IN44	GEM	169.8	3580
436	IN45	x	x	x	Channel Input	IN45	GEM	169.8	3640
437	IN46	x	x	x	Channel Input	IN46	GEM	169.8	3700
438	IN47	x	x	x	Channel Input	IN47	GEM	169.8	3760
439	IN48	x	x	x	Channel Input	IN48	GEM	169.8	3820
440	IN49	x	x	x	Channel Input	IN49	GEM	169.8	3880
441	IN50	x	x	x	Channel Input	IN50	GEM	169.8	3940
442	IN51	x	x	x	Channel Input	IN51	GEM	169.8	4000
443	IN52	x	x	x	Channel Input	IN52	GEM	169.8	4060
444	IN53	x	x	x	Channel Input	IN53	GEM	169.8	4120
445	IN54	x	x	x	Channel Input	IN54	GEM	169.8	4180
446	IN55	x	x	x	Channel Input	IN55	GEM	169.8	4240
447	IN56	x	x	x	Channel Input	IN56	GEM	169.8	4300
448	IN57	x	x	x	Channel Input	IN57	GEM	169.8	4360
449	IN58	x	x	x	Channel Input	IN58	GEM	169.8	4420
450	IN59	x	x	x	Channel Input	IN59	GEM	169.8	4480
451	IN60	x	x	x	Channel Input	IN60	GEM	169.8	4540
452	IN61	x	x	x	Channel Input	IN61	GEM	169.8	4600
453	IN62	x	x	x	Channel Input	IN62	GEM	169.8	4660
454	IN63	x	x	x	Channel Input	IN63	GEM	169.8	4720
455	IN64	x	x	x	Channel Input	IN64	GEM	169.8	4780
456	IN65	x	x	x	Channel Input	IN65	GEM	169.8	4840
457	IN66	x	x	x	Channel Input	IN66	GEM	169.8	4900
458	IN67	x	x	x	Channel Input	IN67	GEM	169.8	4960
459	IN68	x	x	x	Channel Input	IN68	GEM	169.8	5020
460	IN69	x	x	x	Channel Input	IN69	GEM	169.8	5080
461	IN70	x	x	x	Channel Input	IN70	GEM	169.8	5140
462	IN71	x	x	x	Channel Input	IN71	GEM	169.8	5200
463	IN72	x	x	x	Channel Input	IN72	GEM	169.8	5260
464	IN73	x	x	x	Channel Input	IN73	GEM	169.8	5320
465	IN74	x	x	x	Channel Input	IN74	GEM	169.8	5380
466	IN75	x	x	x	Channel Input	IN75	GEM	169.8	5440
467	IN76	x	x	x	Channel Input	IN76	GEM	169.8	5500
468	IN77	x	x	x	Channel Input	IN77	GEM	169.8	5560
469	IN78	x	x	x	Channel Input	IN78	GEM	169.8	5620
470	IN79	x	x	x	Channel Input	IN79	GEM	169.8	5680
471	IN80	x	x	x	Channel Input	IN80	GEM	169.8	5740
472	IN81	x	x	x	Channel Input	IN81	GEM	169.8	5800
473	IN82	x	x	x	Channel Input	IN82	GEM	169.8	5860
474	IN83	x	x	x	Channel Input	IN83	GEM	169.8	5920
475	IN84	x	x	x	Channel Input	IN84	GEM	169.8	5980
476	IN85	x	x	x	Channel Input	IN85	GEM	169.8	6040
477	IN86	x	x	x	Channel Input	IN86	GEM	169.8	6100
478	IN87	x	x	x	Channel Input	IN87	GEM	169.8	6160
479	IN88	x	x	x	Channel Input	IN88	GEM	169.8	6220
480	IN89	x	x	x	Channel Input	IN89	GEM	169.8	6280
481	IN90	x	x	x	Channel Input	IN90	GEM	169.8	6340
482	IN91	x	x	x	Channel Input	IN91	GEM	169.8	6400
483	IN92	x	x	x	Channel Input	IN92	GEM	169.8	6460
484	IN93	x	x	x	Channel Input	IN93	GEM	169.8	6520
485	IN94	x	x	x	Channel Input	IN94	GEM	169.8	6580
486	IN95	x	x	x	Channel Input	IN95	GEM	169.8	6640
487	IN96	x	x	x	Channel Input	IN96	GEM	169.8	6700
488	IN97	x	x	x	Channel Input	IN97	GEM	169.8	6760
489	IN98	x	x	x	Channel Input	IN98	GEM	169.8	6820
490	IN099	x	x	x	Channel Input	IN099	GEM	169.8	6880
491	IN100	x	x	x	Channel Input	IN100	GEM	169.8	6940
492	IN101	x	x	x	Channel Input	IN101	GEM	169.8	7000
493	IN102	x	x	x	Channel Input	IN102	GEM	169.8	7060
494	IN103	x	x	x	Channel Input	IN103	GEM	169.8	7120
495	IN104	x	x	x	Channel Input	IN104	GEM	169.8	7180
496	IN105	x	x	x	Channel Input	IN105	GEM	169.8	7240
497	IN106	x	x	x	Channel Input	IN106	GEM	169.8	7300
498	IN107	x	x	x	Channel Input	IN107	GEM	169.8	7360
499	IN108	x	x	x	Channel Input	IN108	GEM	169.8	7420
500	IN109	x	x	x	Channel Input	IN109	GEM	169.8	7480
501	IN110	x	x	x	Channel Input	IN110	GEM	169.8	7540
502	IN111	x	x	x	Channel Input	IN111	GEM	169.8	7600
503	IN112	x	x	x	Channel Input	IN112	GEM	169.8	7660
504	IN113	x	x	x	Channel Input	IN113	GEM	169.8	7720
505	IN114	x	x	x	Channel Input	IN114	GEM	169.8	7780
506	IN115	x	x	x	Channel Input	IN115	GEM	169.8	7840
507	IN116	x	x	x	Channel Input	IN116	GEM	169.8	7900
508	IN117	x	x	x	Channel Input	IN117	GEM	169.8	7960
509	IN118	x	x	x	Channel Input	IN118	GEM	169.8	8020
510	IN119	x	x	x	Channel Input	IN119	GEM	169.8	8080
511	IN120	x	x	x	Channel Input	IN120	GEM	169.8	8140
512	IN121	x	x	x	Channel Input	IN121	GEM	169.8	8200
513	IN122	x	x	x	Channel Input	IN122	GEM	169.8	8260
514	IN123	x	x	x	Channel Input	IN123	GEM	169.8	8320
515	IN124	x	x	x	Channel Input	IN124	GEM	169.8	8385
516	IN125	x	x	x	Channel Input	IN125	GEM	169.8	8455
517	IN126	x	x	x	Channel Input	IN126	GEM	169.8	8535
518	IN127	x	x	x	Channel Input (MSB first bit in data packet)	IN127	GEM	169.8	8625
519	IN128	x	x	x	Test Channel Input	IN128	Icmo	169.8	8745

TP_ADC_SOC_pad
TP_ADC_CTRL_pad<0>
TP_ADC_CTRL_pad<1>
TP_DF_DTS_pad
TP_DF_TXD_pad<7>
TP_DF_TXD_pad<6>
TP_DF_TXD_pad<5>
VSS
VDD_IO
VDD
VDD
VSS
VSS
TP_DF_TXD_pad<4>
TP_DF_TXD_pad<3>
TP_DF_TXD_pad<2>
TP_DF_TXD_pad<1>
TP_DF_TXD_pad<0>
TP_DF_CTRL_pad<0>
TP_DF_CTRL_pad<1>
TP_CL_CAL_pad
TP_CL_LV1A_pad
TP_CL_RESYNC_pad
TP_CL_BC0_pad
TP_CL_EC0_pad
TP_CL_CTRL_pad<0>
TP_CL_CTRL_pad<1>
SPI_DO_pad
SPI_DI_pad
SPI_EN_pad
SPI_CLK_pad
SCAN_CLK0_EN_pad
SCAN_CLK0_pad
VSS
VDD_EFUSE
VDD_IO
VSS
VSS
VSS
VDD
VDD
VDD_SLVS
VSS
TU_SoT_p
TU_SoT_n
TU_TXD_p<0>
TU_TXD_n<0>
TU_TXD_p<1>
TU_TXD_n<1>

VDD_IO
VSS
VSS
VSS
VDD
VDD
VDD_SLVS
VSS
TU_SoT_p
TU_SoT_n
TU_TXD_p<0>
TU_TXD_n<0>
TU_TXD_p<1>
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TU_TXD_n<2>
TU_TXD_p<3>
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TU_TXD_n<4>
TU_TXD_p<5>
TU_TXD_n<5>
TU_TXD_p<6>
TU_TXD_n<6>
TU_TXD_p<7>
TU_TXD_n<7>
TXD_p
TXD_n
RXD_p
RXD_n
RXCLK_p
RXCLK_n
VDD_SLVS
VSS
VDD
VDD
VSS
VSS

13.   REFERENCES

[1] M.Firlej, T.Fiutowski, M.Idzik, J.Moron, K.Swientek. A fast multichannel, ultra-low power 10-bit ADC for readout of future particle physics detectors, Twepp2015 IST Lisbon Portugal