IP-OCTAL-485

Eight Channel Asynchronous Serial RS-485 IndustryPack®

User Manual

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IP-Octal-485
Eight Channel Asynchronous
Serial RS-485
IndustryPack®

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Product Description

IP-OCTAL-485 is part of the Industry Pack™ family of modular I/O components. It is based around the Signetics CMOS SCC2698 Octal Universal Asynchronous Receiver/Transmitter. This component provides eight channels of full-duplex asynchronous serial communications, baud rate generators, state change detect logic, and four 16-bit counter/timers.

A block diagram of the IP-OCTAL-485 is shown below in Figure 1.

RS-485 communication levels are provided by 75LBC176 differential transceivers. Differential bidirectional (DxD) lines are provided, plus ground. In addition to being bidirectional, i.e. supporting multidrop topologies, RS-485 communication is preferred over RS-232 because it provides significantly higher noise immunity. Another advantage is that no ±12 volt power is required at either the send or receive end.

Vectored interrupts are fully supported. A common 8-bit vector register is provided. Channels a,b,c,d interrupt on IRQ0. Channels e,f,g,h interrupt on IRQ1.

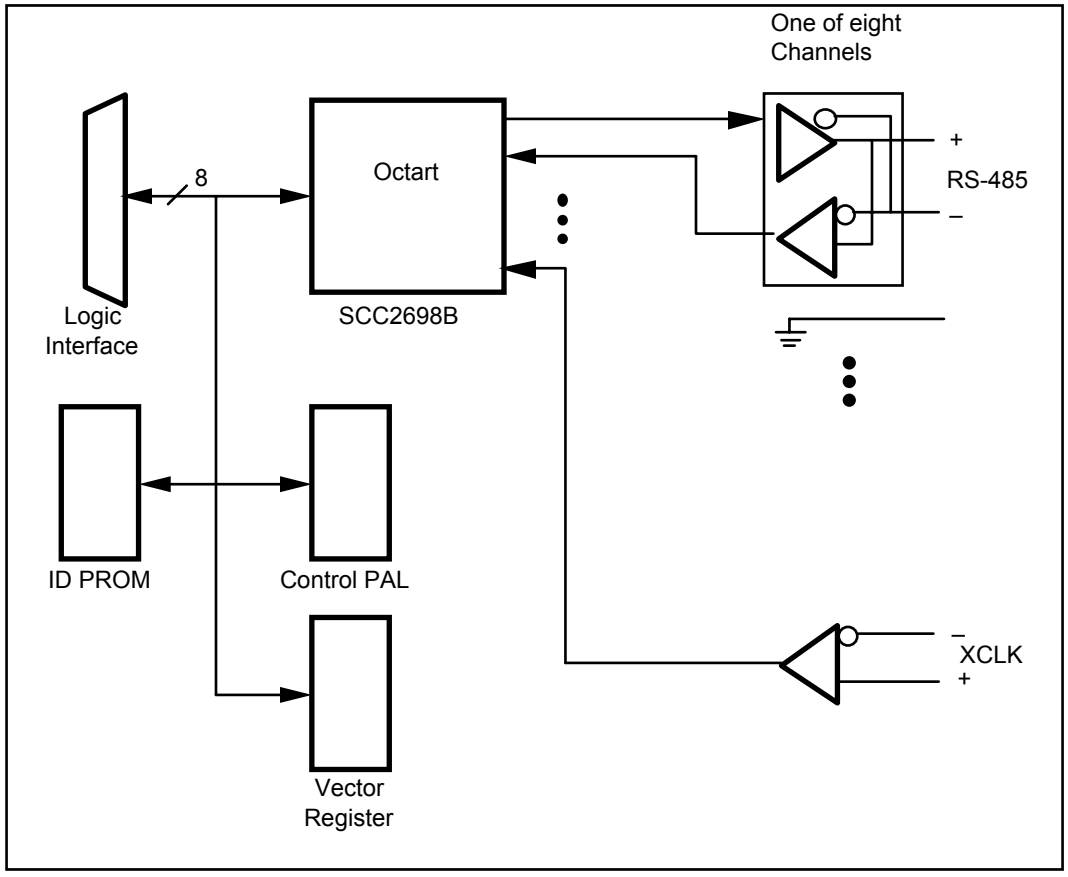

Figure 1 Simplified Block Diagram of IP-OCTAL-485

The IndustryPack is controlled by a single CMOS 22V10 type PAL.

Connection to the IP-OCTAL-485 is via a standard 50-conductor ribbon cable. An optional connection panel is available which provides a 50-pin flat cable input with 16 DB-9 male or female connectors. The metal reinforced connection panel mounts in a standard 19 inch rack-mount space.

VMEbus Addressing

IP-OCTAL-485 is accessed using 8-bit bytes at odd locations only. It is usually accessed in the I/O space. Shown below in Figures 2 and 3 are the register maps of the IP-OCTAL-485. All addresses are offsets from the I/O base address of the IP as set on the IP carrier board.

The SCC2698B Octal UART has four major internal sections, called functional blocks A through D. Each functional block has two serial channels, one timer, and one I/O port.

Hex	Dec	Binary	Read	Write
		Functional Block A		
1	1	0000001	MR1a, MR2a	MR1a, MR2a
3	3	0000011	SRa	CSRa
5	5	0000101	RESERVED	CRa
7	7	0000111	RHRa	THRa
9	9	0001001	IPCRA	ACRA
B	11	0001011	ISRA	IMRA
D	13	0001101	CTUA	CTURA
F	15	0001111	CRLB	CTLRB
11	17	0010001	MR1b, MR2b	MR1b, MR2b
13	19	0010011	SRb	CSRb
15	21	0010101	RESERVED	CRb
17	23	0010111	RHRb	RHRb
19	25	0011001	RESERVED	RESERVED
1B	27	0011011	INPUT PORT A	OPCRA
1D	29	0011101	START C/T A	RESERVED
1F	31	0011111	STOP C/T A	RESERVED
		Functional Block B		
21	33	0100001	MR1c, MR2c	MR1c, MR2c
23	35	0100011	SRc	CSRc
25	37	0100101	RESERVED	CRc
27	39	0100111	RHRc	THRc
29	41	0101001	IPCRB	ACRB
2B	43	0101011	ISRB	IMRB
2D	45	0101101	CTUB	CTURB
2F	47	0101111	CRLB	CTLRB
31	49	0110001	MR1d, MR2d	MR1d, MR2d
33	51	0110011	SRd	CSRd
35	53	0110101	RESERVED	CRd
37	55	0110111	RHRd	THRd
39	57	0111001	RESERVED	RESERVED
3B	59	0111011	INPUT PORT B	OPCRB
3D	61	0111101	START C/T B	RESERVED
3F	63	0111111	STOP C/T B	RESERVED

Figure 2 Register Map of SCC2698, Blocks A and B

Hex	Dec	Binary	Read	Write
		Functional Block C		
41	65	1000001	MR1e, MR2e	MR1e, MR2e
43	67	1000011	SRe	CSRe
45	69	1000101	RESERVED	CRe
47	71	1000111	RHRe	THRe
49	73	1001001	IPCRC	ACRC
4B	75	1001011	ISRC	IMRC
4D	77	1001101	CTUC	CTURC
4F	79	1001111	CRLC	CTLRC
51	81	1010001	MR1f, MR2f	MR1f, MR2f
53	83	1010011	SRf	CSRf
55	85	1010101	RESERVED	CRf
57	87	1010111	RHRf	THRf
59	89	1011001	RESERVED	RESERVED
5B	91	1011011	INPUT PORT C	OPCRC
5D	93	1011101	START C/T C	RESERVED
5F	95	1011111	STOP C/T C	RESERVED
		Functional Block D		
61	97	1100001	MR1g, MR2g	MR1g, MR2g
63	99	1100011	SRg	CSRg
65	101	1100101	RESERVED	CRg
67	103	1100111	RHRg	THRg
69	105	1101001	IPCRD	ACRD
6B	107	1101011	ISRD	IMRD
6D	109	1101101	CTUD	CTURD
6F	111	1101111	CRLD	CTLRD
71	113	1110001	MR1h, MR2h	MR1h, MR2h
73	115	1110011	SRh	CSRh
75	117	1110101	RESERVED	CRh
77	119	1110111	RHRh	RHRh
79	121	1111001	RESERVED	RESERVED
7B	123	1111011	INPUT PORT D	OPCRD
7D	125	1111101	START C/T D	RESERVED
7F	127	1111111	STOP C/T D	RESERVED

Figure 3 Register Map of SCC2698, Blocks C and D

For NuBus applications see the section following, Nubus Addressing.

NuBus Addressing

Since the Nubus uses only 32-bit wide accesses, 8-bit wide peripherals such as the IP-OCTAL-485 appear in the host address space every fourth byte.

To calculate the RM1260 Springboard register addresses from the VMEbus address (given in the previous section in Figures 2 and 3), multiply by two and subtract one. To convert VME addresses to RM1270 SupportBoard addresses multiply by two and add one.

I/O Pin Assignments

This section gives the pin assignments for IP-OCTAL-485 connections.

Pin Number	Channel	Function	Level
1	Channel a	GND	RS-485
2	Channel a	Dx–	RS-485
3	Channel a	Dx+	RS-485
4	-	no connection	
5	-	no connection	
6	Channel b	GND	RS-485
7	Channel b	Dx–	RS-485
8	Channel b	Dx+	RS-485
9	-	no connection	
10	-	no connection	
11	Channel c	GND	RS-485
12	Channel c	Dx–	RS-485
13	Channel c	Dx+	RS-485
14	-	no connection	
15	-	no connection	
16	Channel d	GND	RS-485
17	Channel d	Dx–	RS-485
18	Channel d	Dx+	RS-485
19	-	no connection	
20	-	no connection	
21	Channel e	GND	RS-485
22	Channel e	Dx–	RS-485
23	Channel e	Dx+	RS-485
24	-	no connection	
25	-	no connection	
26	Channel f	GND	RS-485
27	Channel f	Dx–	RS-485
28	Channel f	Dx+	RS-485
29	-	no connection	
30	-	no connection	
31	Channel g	GND	RS-485
32	Channel g	Dx–	RS-485
33	Channel g	Dx+	RS-485
34	-	no connection	
35	-	no connection	
36	Channel h	GND	RS-485
37	Channel h	Dx–	RS-485
38	Channel h	Dx+	RS-485
39	-	XClk-	RS-422/TTL
40	-	XClk+	RS-422/TTL
41	--	GND	--
42	--	no connection	
43	-	no connection	
44	-	no connection	
45	-	no connection	
46	-	no connection	
47	-	no connection	
48	-	no connection	
49	-	no connection	
50	-	no connection	

Figure 4 I/O Pin Assignment

Each channel has three lines. Each channel is wired identically at the 50-pin connector. The three lines are Ground, Data input/output Minus, Data input/output Plus. The common ground line for all channels connects to the local logic ground. RS485 termination resistors have been provided for each channel. These resistors may or may not be required depending upon RS485 network topology and channel position within that topology. For this reason, the resistors are contained within socketed R-packs to facilitate user removal. See User Options section for details.

Provision for external clock input is made available on pins 39 and 40. The external clock may be either RS422 or standard TTL logic levels. If TTL inputs are used, configuration shunt E1 must be installed. If RS422 inputs are used, E1 is not installed but RS422 terminating resistor R8 must be installed.

IndustryPack Logic Interface Pin Assignment

Figure 5 below gives the pin assignments for the IndustryPack Logic Interface on the IP-OCTAL-485. Pins marked n/c below are defined by the specification, but not used on IP-OCTAL-485.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSel*	4	29
D1	DMAReq0	5	30
D2	MEMSel*	6	31
D3	DMAReq1	7	32
D4	INTSel*	8	33
D5	DMAck0*	9	34
D6	IOSel*	10	35
D7	DMAck1*	11	36
n/c	A1	12	37
n/c	n/c	13	38
n/c	A2	14	39
n/c	n/c	15	40
n/c	A3	16	41
n/c	n/c	17	42
n/c	A4	18	43
n/c	n/c	19	44
n/c	A5	20	45
n/c	Strobe*	21	46
–12V	A6	22	47
+12V	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 5 Logic Interface Pin Assignment

Programming

The IP-OCTAL-485 is designed around the SCC2698B and all of the SCC2698 functions are available. The SCC2698B is divided into four Functional Blocks lettered A through D. Each functional block contains two serial channels. The channels are identified by lower case letters a through h. The SCC2698B contains 64 internal registers, 16 for each functional block. Each of these registers are accessible using a read or write to the IP-OCTAL-485 I/O space. The SCC2698 manual provides the user with detailed information about these registers.

Transceiver direction control for each channel is accomplished by progrmming the Multi-Purpose Output (MPOa-MPOh) pin as the Request to Send. function. See the SCC2698 manual for specific details and the various Request to Send control options available.

The IndustryPack provides an external vector register. The address of the vector register, which may also be read normally, is in the upper half of the ID PROM space of the IndustryPack, on odd bytes. The address offsets are shown in Figure 6.

There is also provision for mapping the vector register to IP memory space. This is required primarily when the IP is installed on a Motorola MVME62 CPU board. In this mode, no address offset is required; the memory base address is sufficient.

Carrier	Bus	Address
VIPC310	VMEbus	IP I/O base + $C1
VIPC610	VMEbus	IP I/O base + $C1
MVME162	IPIC	IP Memory base
RM1260	NuBus	IP ID base + $81
RM1270	NuBus	IP ID base + $83

Figure 6 Location of the Vector Register

The eight bit vector is loaded by the host software prior to enabling interrupts. The interrupts service routine polls the SCC2698B to determine the detailed cause of the interrupt. Function Blocks A and B interrupt on IRQ0. Function Blocks C and D interrupt on IRQ1. See the User Manual for your IP Carrier tor interrupt mapping to your bus. Note that although two distinct interrupt levels are provided, there is a single vector for the IndustryPack.

ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

Standard data in the ID PROM on the IP-OCTAL-485 is shown in Figure 7 below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from SBS Technologies.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure 7 below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

The ID PROM used is an AMD 27LS19A or equivalent.

3F 19	(available for user)	
17	CRC	
15	No of bytes used	(0B)
13	Driver ID, high byte	
11	Driver ID, low byte	
0F	reserved	(00)
0D	Revision	(A1)
0B	Model No IP-OCTAL-485	(48)
09	Manufacturer ID GreenSpring	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 7 ID PROM Data (hex)

User Options

There is only one configuration shunt on the IP, E1.

Provision for selection of an internal or external clock source to the 2698. For standard configurations, the clock is external and is made available on pins 39 and 40 of the IP I/O connector. The external clock may be either RS422 or standard TTL logic levels. If TTL inputs are used, configuration shunt E1 must be installed. If RS422 inputs are used, E1 is not installed but RS422 terminating resistor R8 must be installed.

An on-board oscillator U16 is available for special order configurations only.

Clock Source	Level	Shunt E1	Osc U16	Term. R8
Internal	Logic	Not installed	Installed	-
External	Logic	Installed	Not installed	Not installed
External	RS422	-	Not installed	Installed

Figure 8 Clock Source Options

In RS485 multi-point differential bus configurations, only two of the attached channels should provide termination: those physically positioned at either end of the network. Figure 10 shows a multipoint configuration illustrating the maximum of 32 unit loads as specified by Electrical Characteristics Standard TIA/EIA-485. Termination resistors Rt are shown at points T1 and T2 only. RS485 termination resistor value is 120Ω. Also shown in Figure 10 and provided for on IP-OCTAL-485 is a failsafe biasing resistive network consisting of two resistors, each 750Ω in value, with one attached to Vcc and the other to ground. The purpose of failsafe biasing is to establish a known state on the bus when all the drivers are in tri-state (off). Failsafe biasing resistors are only required on one channel within the configuration.

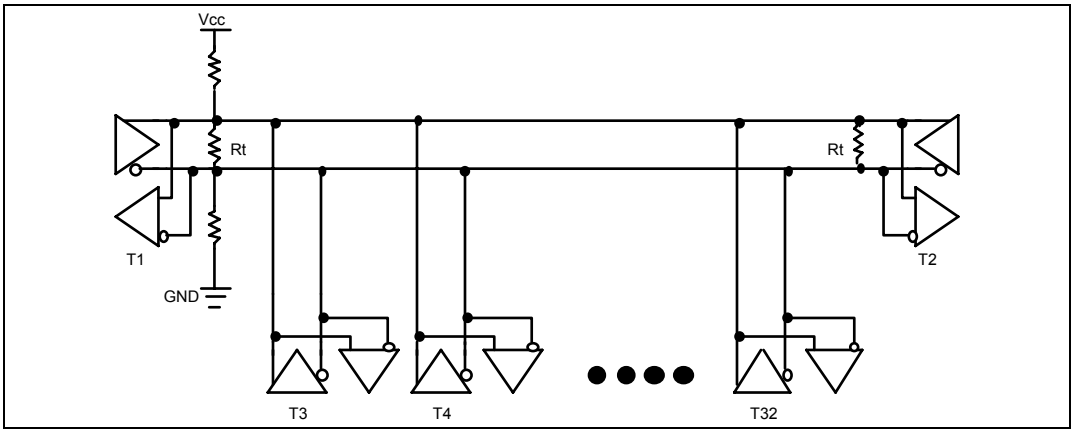

Figure 9 RS485 Multipoint Termination

Socketed Resistor Packs RP1 and RP2 provide RS485 termination resistors for each of the eight data channels. RP1 corresponds to channels A,B,C, and D, and RP2 corresponds to channels E,F,G, and H. See Figure 9 for specific pin/signal assignments. Removal of the termination resistors for non-terminating channels can be achieved by removing the RP, cutting off the appropriate pin leads, and reinstalling RP in the socket. Obviously if all four channels connected to a given RP are non-terminating channels, the RP can simply be removed and discarded.

Resistor Pack	Pin	Channel	Signal
RP1	1	a	Dx–
RP1	2	a	Dx+
RP1	3	b	Dx–
RP1	4	b	Dx+
RP1	5	c	Dx–
RP1	6	c	Dx+
RP1	7	d	Dx–
RP1	8	d	Dx+
RP2	1	e	Dx–
RP2	2	e	Dx+
RP2	3	f	Dx–
RP2	4	f	Dx+
RP2	5	g	Dx–
RP2	6	g	Dx+
RP2	7	h	Dx–
RP2	8	h	Dx+

Figure 10 RS485 Terminators

Resistor Packs RP3 and RP4 provide RS485 failsafe biasing resistors for each of the eight data channels. RP3 connects the plus side of each driver to Vcc; RP4 connects the minus side of each driver to ground. See Figure 10 for specific pin/signal assignments. Removal of the failsafe biasing resistors can be achieved by removing the RP, cutting off the appropriate pin leads, and reinstalling the RP in the socket. Obviously if none of the channels on the IP require failsafe biasing resistors, the RPs can simply be removed and discarded.

Resistor Pack	Pin	Channel	Signal
RP3	2	a	Dx+
RP3	3	b	Dx+
RP3	4	c	Dx+
RP3	5	d	Dx+
RP3	6	e	Dx+
RP3	7	f	Dx+
RP3	8	g	Dx+
RP3	9	h	Dx+
RP4	2	a	Dx–
RP4	3	b	Dx–
RP4	4	c	Dx–
RP4	5	d	Dx–
RP4	6	e	Dx–
RP4	7	f	Dx–
RP4	8	g	Dx–
RP4	9	h	Dx–

Figure 11 RS485 Biasing Resistors

Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-OCTAL-485 is constructed out of 0.062 inch thick FR4 material. The six copper layers consist of a ground plane, a power plane and four signal planes.

Surface mounting of components is used extensively. IC sockets for the control PAL and ID PROM use gold plated screw-machined pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is optionally secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

Repair

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the factory for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS Technologies will not be responsible for damages due to improper packaging of returned items.

Shunt Locations

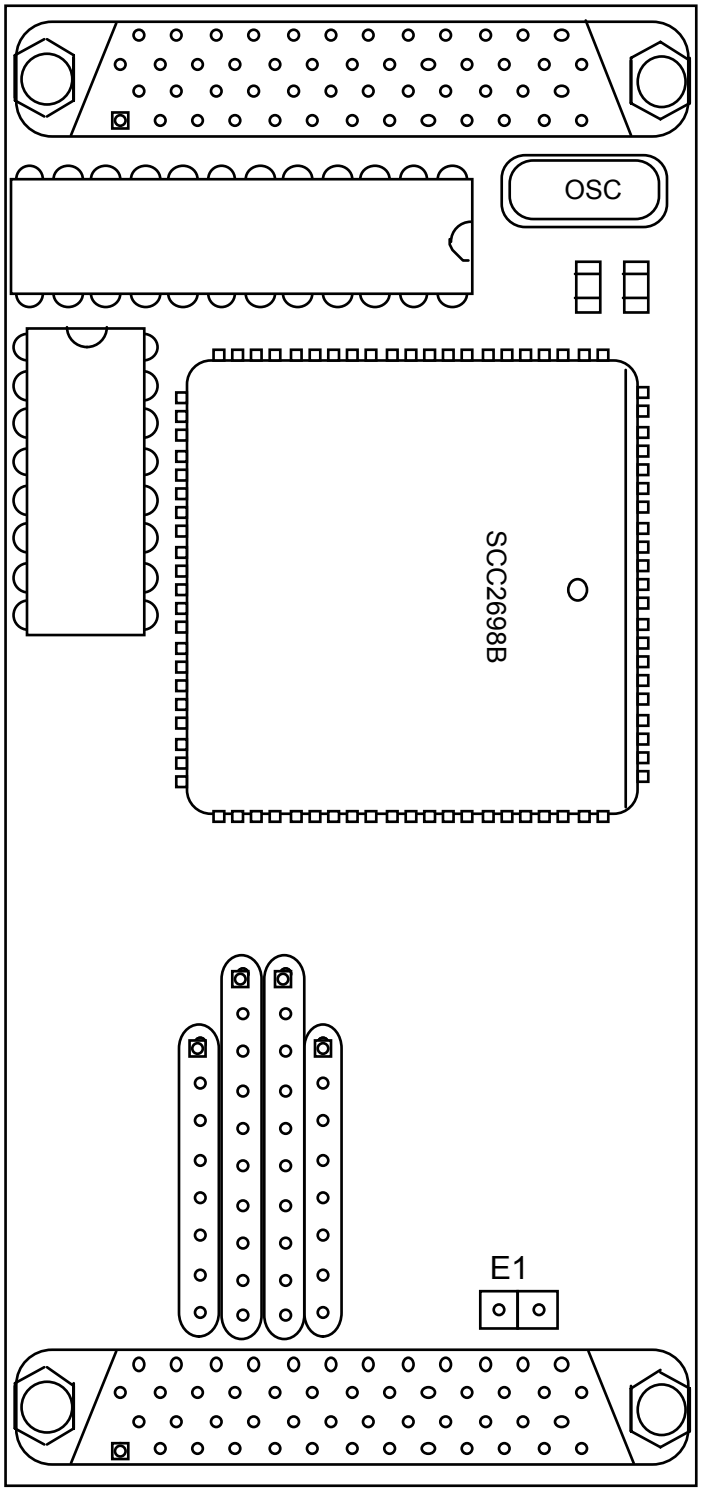

Figure 12 Shunt Locations

Specifications

Logic Interface	IndustryPack logic Interface
Wait States	Zero on ID and Interrupts, One on SCC accesses
Number of Channels	Eight
Type of Channels	Half-duplex asynchronous RS-485
Baud Rates	18 fixed rates from 50 to 38.4K Four user-defined rates using timers
Implemented Signals	Dx+, Dx–, GND
Stop Bits	1, 1.5, 2 in 1/16 bit increments
Clock Source	Local crystal oscillator, or external
Error Detection	Parity, framing, overrun, false start bit, break
Channel Modes	Half duplex, automatic echo, local loopback, remote loopback
Number of Timers	Four
Type of Timers	16-bit, multi-function, programmable
Interrupt Sources	32, maskable, vectored
Interrupt Vector	8 bits, may be independently read/writable
Auxiliary Input lines	8 TTL/CMOS level inputs, programmable bit input or state change detect causes interrupt or counter/external clock input
IP Strobe Options	Timer output, baud rate clock input, or none
Power Requirements	+5 VDC, 285 mA, typical +12 VDC, 0 mA –12 VDC, 0 mA
Dimensions	1.800 by 3.900 by 0.340 inches maximum
Environmental	Operating temperature: 10 to 50°C Humidity: 5 to 95% non-condensing Storage: –10 to +85°C