Extended baud rates for SCN2681, SCN68681, SCC2691, SCC2692, SCC68681 and SCC2698B

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1991 April 04

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AFFECT OF ‘RESERVED REGISTERS’ ON BAUD RATES

The Philips Semiconductors UART chips (EXCEPTING the SC26C94) all have two test modes which are accessed via a READ of the reserved registers at hex address 2 and A. Each time a read of either address is performed, a flip-flop at that address will toggle. Software must keep track of the state of these flop-flops since there is no internal indication of the sate of these flop-flops. They are reset to the non-test condition by a hardware reset of the chip. Other methods for resetting are described below.

The test mode at address 2 is useful for the user requiring higher speed baud rates. It gives rates up to 115.2Kb in the 16x mode. In test mode 2 the dividers in the baud rate generator are changed. Test mode 2 will, therefore, effect all UARTs on the chip. Please note in the table below that some of the more common baud rates do not change when in test mode 2. Test 2 also changes the RTSN outputs to the transmitter 1x clock.

Table 1. Baud Rates

Test 2 = 0	Test 2 = 1	Test 2 = 1	Test 2 = 0
Test A = 0	Test A = 0	Test A = 1	Test A = 1
1x Baud Rate	1x Baud Rate	1x Baud Rate	1x Baud Rate
38,400	38,400	614,400	614,400
19,200	19,200	307,200	307,200
9,600	9,600	153,600	153,600
7,200	57,600	921,600	115,200
4,800	4,800	76,800	76,800
2,400	57,600	921,600	38,400
2,000	2,000	32,000	32,000
1,800	14,400	230,400	28,800
1,200	115,200	1,843,200	19,200
1,050	1,050	16,800	16,800
600	57,600	921,600	9,600
300	28,800	460,800	4,800
200	19,200	307,200	3,200
150	14,400	230,400	2,400
134.5	1,076	17,216	2,152
110	880	14,080	1,760
75	7,200	115,200	1,200
50	4,800	76,800	800

The baud rate of 115,200 would be selected by first reading address 2 and then setting the CSR (Clock Select Register) for the 1200 baud rate.

The test mode at address A changes all receivers and transmitters to the 1x mode of operation. It also connects some of the output pins to to various internal signals (mostly baud rate clocks). This mode is not very useful unless the 1x mode is desired for all channels and the output port pins are not used. Use of the test mode will not violate any of the specified speed parameters. Its use as a normal mode of operation is not, however, specifically verified in productions testing.

As mentioned previously, returning from the test mode to normal operation only requires another read of address 2 or A as appropriate. If for some reason the software is not aware of which test mode is in use, it can be painful to properly reset the test modes since there are four choices of action and only one of them will be correct. Of course a hardware reset will always reset both test modes. Since a hardware reset often is equivalent to a system restart, the following methods are presented to regain control of the test mode.

At the risk of belaboring the subject it should be mentioned that several approaches and several versions of each could be applied – the practicality of each being dependent on the hardware in use. These may be characterized or typed as follows:

1. Internal transmit loop of: send – test – set condition – send ...
2. Use Counter/Timer (C/T) to generate a time period in which a byte or start bit may be sent.
3. Set the C/T to stop upon the completion of transmission. The value in the C/T then directly represents the speed of the unknown data clock. The inverse of 2)
4. Sending data to or receiving data from a known good device and evaluating the error status of that data.

For the discussion below it will be convenient to represent the state of the test flip-flops as two binary bits (00 being normal) thus:

We choose a baud rate which is different for all four conditions of the test bits. The 7200 baud rate is one of these. Any configuration of the test bits except 00 will increase the baud rate by a factor of eight or more. (Specifically 00 = 1x; 01 = 8x; 10 = 1 6x. 11 = 128x). A bit time at 7200 baud is about 138μs and half of that 69μs.

Table 2. Baud Rates

Flip-Flop	Test A	Test 2	7200 Baud Rate
00	inactive	inactive	7200 (normal)
01	inactive	active	57,600
10	active	inactive	115,200
11	active	active	921,000

Type 1.

This method will use features internal to the UART to determine and reset to the normal mode. It will use the counter/timer to set up a known time reference and then read the value of the TxEMT and TxRDY bits in the status register at the end of this time. In normal operation at 7200 baud the A bit time will require 512 clocks of the X1 input. We know that a test mode will increase the 7200 baud rate by at least 8. A bit time then requires 64 ‘X1’ clocks.

Reset receiver and transmitter then set up transmitter for local loop back and 7200 baud. Set counter timer for counter mode, its preset value to 48 (0030 hex), its clock to the X1 input. This C/T setting will cause it to time out at approximately three-fourths bit time. (The precise time is not important nor is the X1 frequency). Interrupt on C/T ready or poll the ISR (Interrupt Status Register) C/T ready bit. The control register setup follows. (Hex values)

13 → MR1 AA → CSR 00 → OPCR 00 → IPCR 00 → CTUR

07 → MR2 4A → CR 60 → ACR 08 → IMR 30 → CTLR

The test loop will look for the TxRDY TxMT status bits to be in the 00 condition when the C/T times out. This will mean that the start bit of a transmitted character has not completed. Since the test modes will, in general, make the data clocks faster by at least a factor of eight, any data clock slower than 2x will cause the above bits to be in the 00 state at C/T time out. The flow would then be:

```
BEGIN
        Toggle Test 2
    TEST ROUTINE:
        Enable Transmitter
        Load Transmit holding register
        Start Counter/timer
        Wait for C/T time out
        Stop C/T
    END TEST
        Read status register, if TxEMT and TxRDY = 00 then quit
        Reset Transmitter
        Toggle Test A
        Call Test Routine
        Read status register, if TxEMT and TxRDY = 00 then quit
        Toggle Test 2

END
```

Assuming the test flop-flops were not in state 00 to begin with, the above will always return the test flip-flops to 00 on or before the second toggle of Test 2. The above is predicated upon knowing the system is in a test condition but not which one. It is therefore valid to guess Test 2 and just blindly toggle that flip-flop as a first step.

Type 2.

Similar to above without TEST ROUTINE and TEST. In this method the value of the C/T will be used to determine an approximate bit rate and from that determine which flip-flops need to be toggled in order to return to normal operation. Since we are dealing with large the baud rate changes that test modes bring about it is not necessary to make exact measurements.

```
Set up the UART as above
        Enable Transmitter
        Load Transmit holding register
        Start Counter/timer
        Wait for C/T time out
        Stop C/T
        Read status register.
```

Depending on the test mode active we would expect the TxEMT TxRDY bits to be as follows:

Table 3.

Test Mode	TxEMT TxRDY
01	00
10	01
11	11

Toggle the test mode bits according to the indication of the transmitter status bits.

Type 3.

Here the value in the C/T is used to determine the active test mode. Preset the C/T to 48 (0030 hex). Set the interrupt for TxRDY. The UART control register settings follow.

13 → MR1 AA → CSR 00 → OPCR 00 → IPCR 00 → CTUR

```
07 → MR2 4A → CR 60 → ACR 01 → IMR 30 → CTLR
        Enable Transmitter
        Load Transmit holding register
        Start Counter/timer
        Wait for TxRDY C/T time out
        Stop C/T
        Read C/T upper and lower registers
```

Table 4.

Counter Value	Indicates Test State
> 512	01 (CTU > 0)
< 16, > 24	10
< 0, > 4	11

The above numbers are based on the time required for a start bit to be sent. Other time intervals of course may be used. The exact values also depend on how fast the control processor can service the interrupts or how long a pooling loop is. One could just as well use a full character time instead of a start bit time.

Type 4.

This test will send a character to a known good receiver. It is suggested to send an eight bit ‘00’ character with even parity at 1800 baud. The test mode will increase the 1800 baud rate to 14400, 230400, or 28800. The UART control register settings follow.

03 → MR1 AA → CSR 00 → OPCR 00 → IPCR 00 → CTUR

07 → MR2 4A → CR EO → ACR 01 → IMR 30 → CTLR

Set the receiver to 9600 baud. Depending on the active test mode and a bit of asynchronous timing the receiver will ‘see’ the 00 character as follows:

Table 5.

Test Mode	Character Received
01	E0 or C0
11	No data received. Byte time shorter than a start bit.
10	FE or FC

The above, of course, may not be very practical when the status of the receiver is not available to the local processor. These have not verified the above in hardware. However, the idea of what is desired is shown. Actual applications will no doubt vary from the above as hardware and system timing dictate

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Date of release: 02-00

Document order number: 9397 750 06852